

Rocket BSW 11.6" Schematic

Braswell

2015-11-09
REV : A00

DY : None Installed
OSP/ISP : different config for storage and DRAM
Drax : stuff on Drax

<Core Design>



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Title

Cover Page

Size
A3

Document Number

Rocket BSW 11.6"

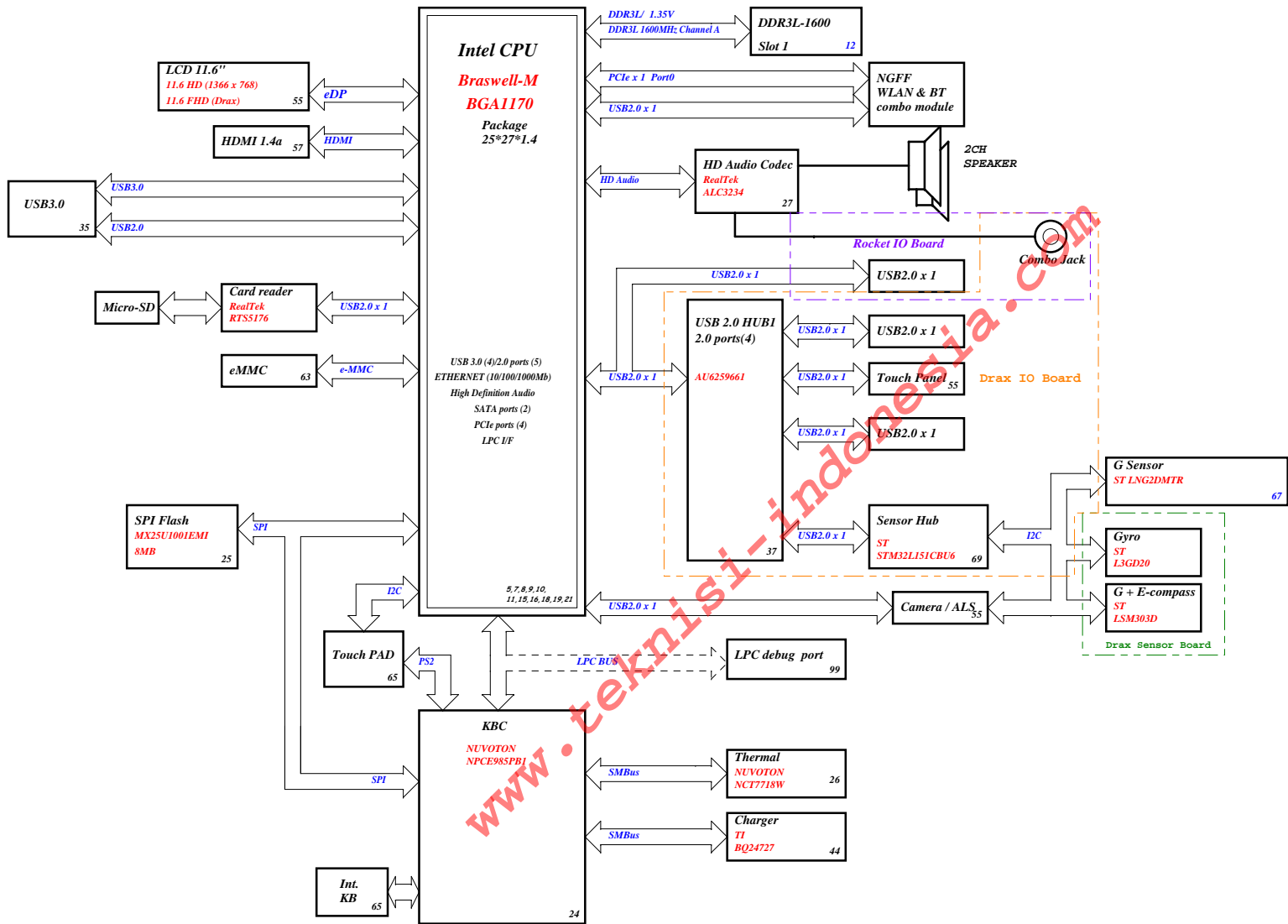
Rev
A00

Date: Tuesday, November 10, 2015

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Project code : 4PD076010001
PCB P/N : 15239
Revision : -1

Rocket 11.6" Block Diagram - 1SP



CHARGER	
BQ24727RGR	44
INPUTS	OUTPUTS
19V_AD+	12V_BT+
SYSTEM DC/DC	
SY8288CRAC	45
SY8286BRAC	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5 5V_S5
CPU DC/DC	
NCP81201MNTXG	46-47
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE
CPU DC/DC	
NCP81201MNTXG	48
INPUTS	OUTPUTS
19V_DCBATOUT	6FX_CORE
SYSTEM DC/DC	
SY8286RAC	50
INPUTS	OUTPUTS
19V_DCBATOUT	1D05V_S5
Step Down Regulator	
SYW232DFC	50
INPUTS	OUTPUTS
3D3V_S5	1D15V_S5
SYSTEM DC/DC	
SY8286RAC	51
INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_CPU_VDDQ_S3
SYSTEM DC/DC	
APL5338XAI	51
INPUTS	OUTPUTS
1D35V_CPU_VDDQ_S3	0D675V_VREF_S0
Step Down Regulator	
SYW232DFC	52
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
SYSTEM LDO	
S-1339D15-M5001	53
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
SYSTEM LDO	
APL5930KAI	54
INPUTS	OUTPUTS
3D3V_S5	1D24V_S5


PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

SSID = CPU

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SSID = CPU

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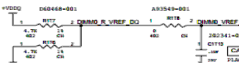
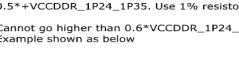
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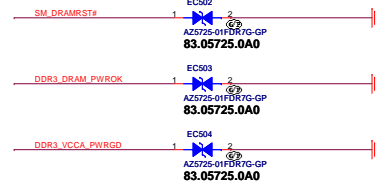
Rev
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Follow Intel Check List, Remove Reference Voltage

<p>DDR3_M0_ODQVREF DDR3_M1_ODQVREF</p>	<p>Not applicable to DDR3L implementation. In DDR3L mode, these pins are No Connect on SoC Vref. External Vref circuitry needs to be given on SODIMM side. Example shown as below</p> <p>0.5*VCCDDR_IP24_IP35. Use 1% resistor. Cannot go higher than 0.6*VCCDDR_IP24_IP35. Example shown as below</p> 	<p>Not use for DDR3L design.</p>
<p>DDR3_M0_OCAVREF DDR3_M1_OCAVREF</p>	<p>Not applicable to DDR3L implementation. In DDR3L mode, these pins are No Connect on SoC Vref. External Vref circuitry needs to be given on SODIMM side. Example shown as below.</p> <p>0.5*+VCCDDR_IP24_IP35. Use 1% resistor. Cannot go higher than 0.6*VCCDDR_IP24_IP35. Example shown as below</p> 	<p>Not use for DDR3L design.</p>



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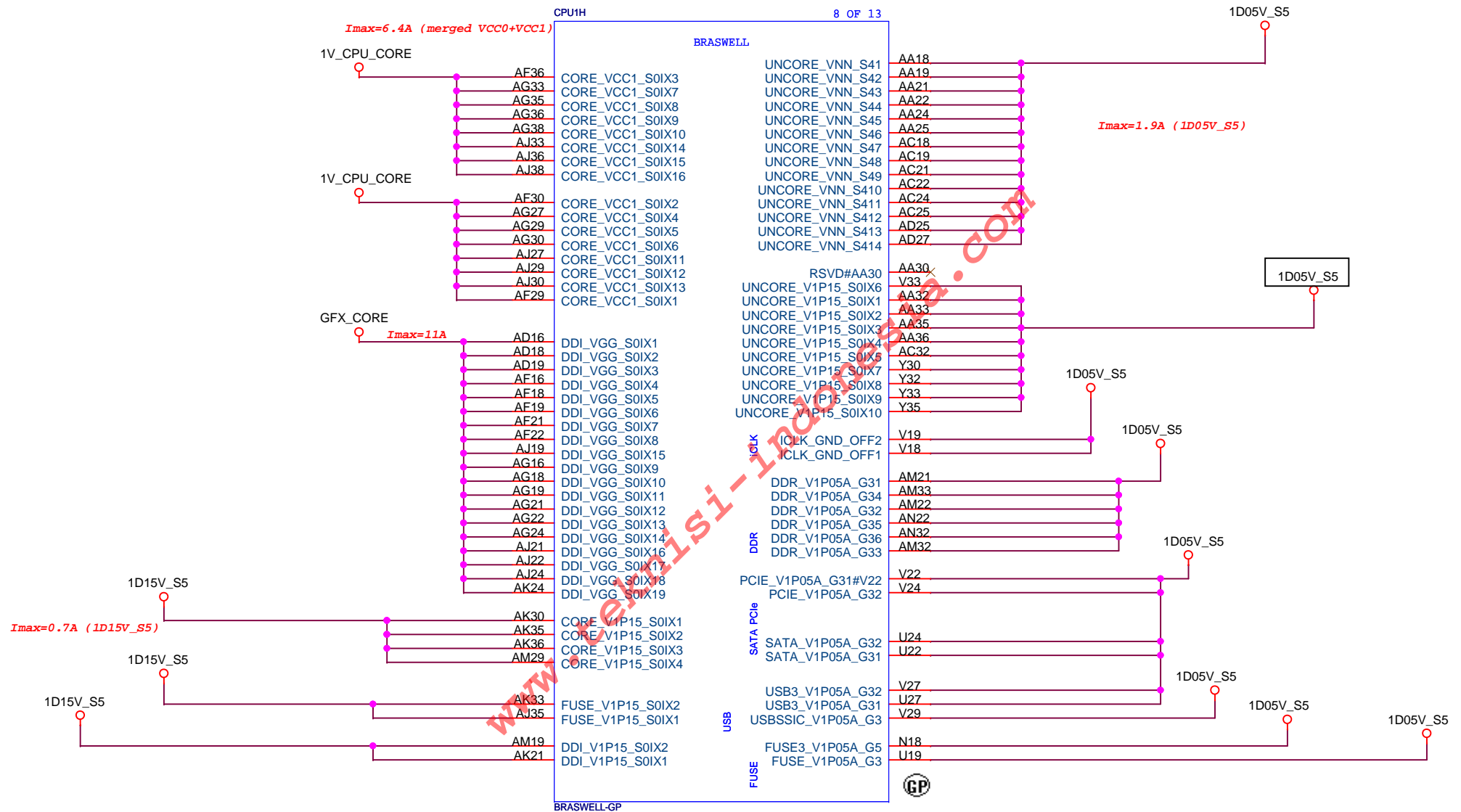
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SSID = CPU



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CPU (VCC CORE)

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Rev

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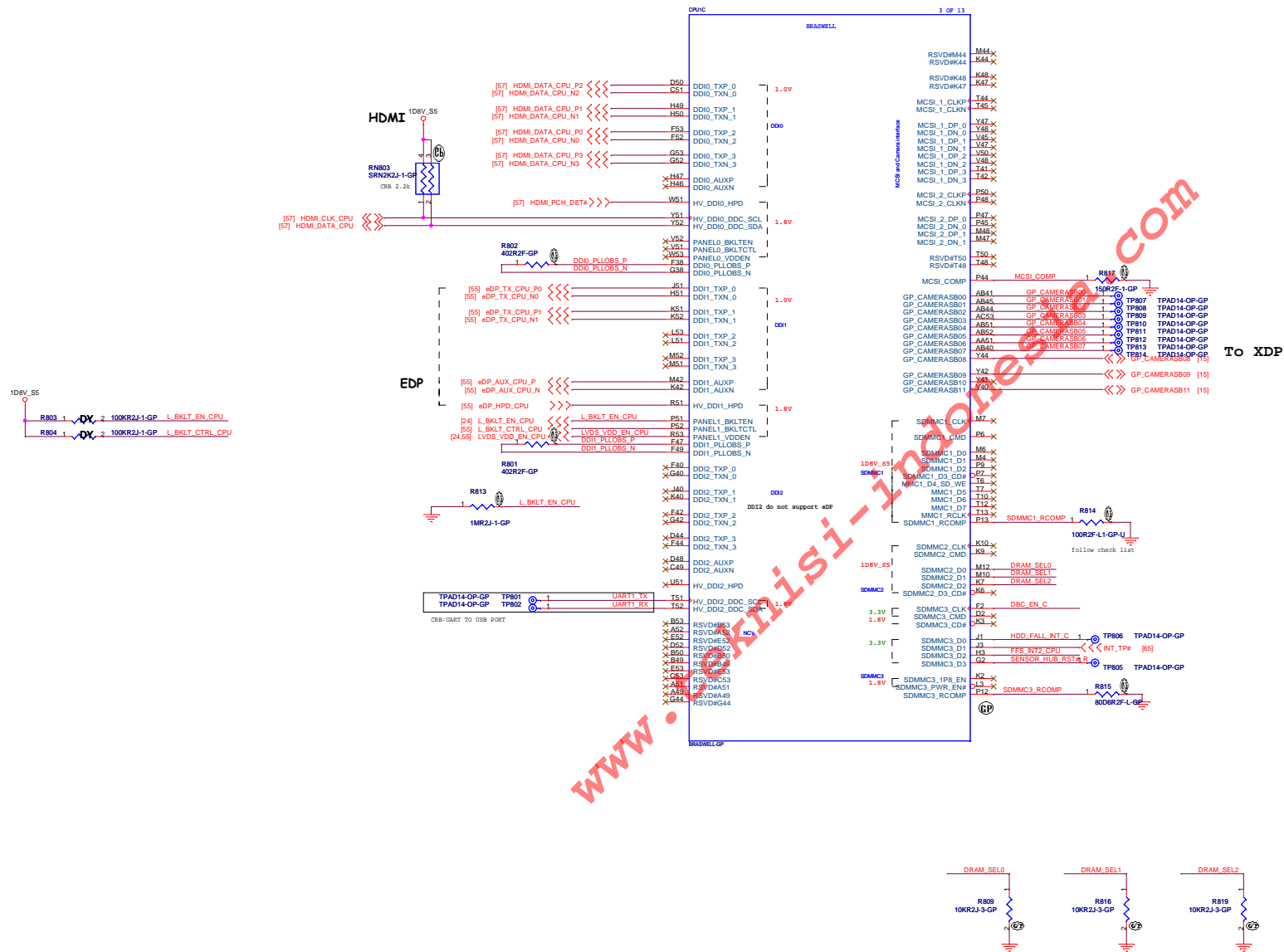
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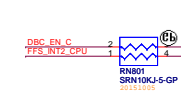
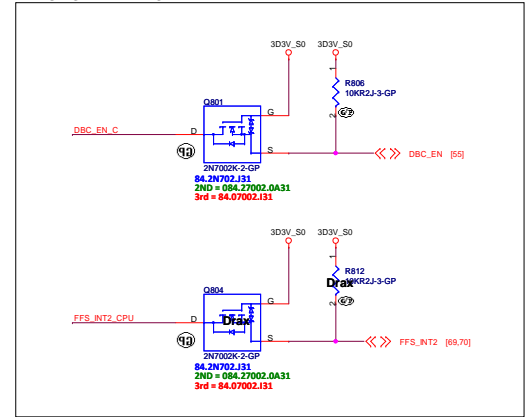
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09

SSID = CPU

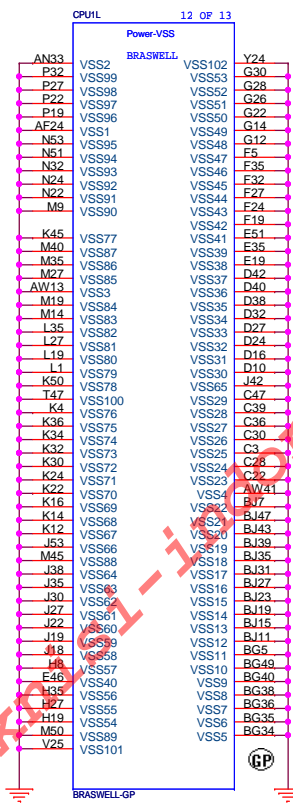
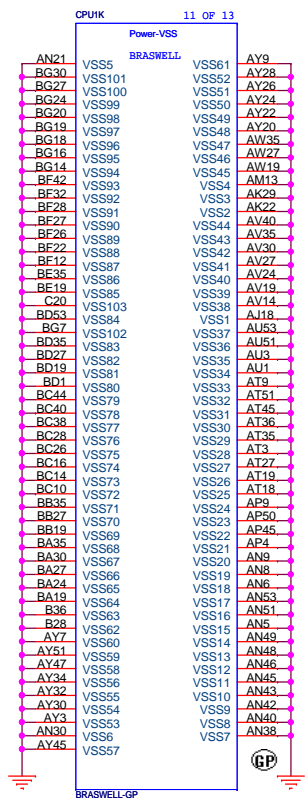
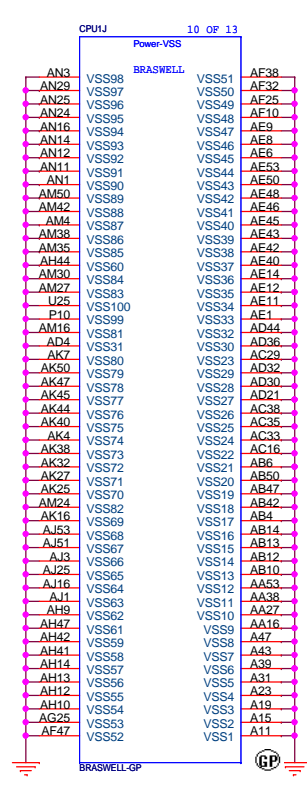


Level Shift



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SSID = CPU



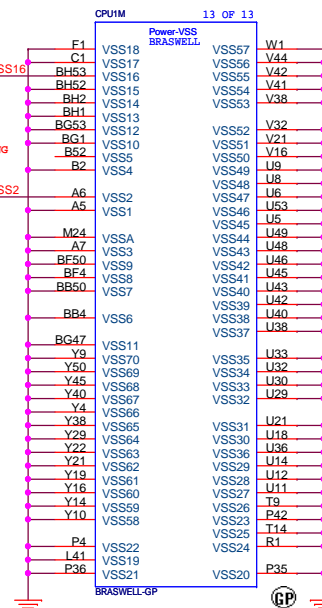
2014/04/25
Intel suggest

TP901 1
TPAD14-OP-GP

2014/04/25
Intel suggest

TP902 1
TPAD14-OP-GP

B52 MAY NOT BE ABLE TO BREAK OUT IN ROUTING



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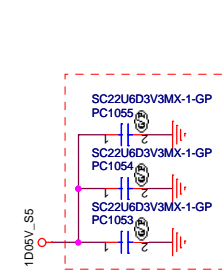
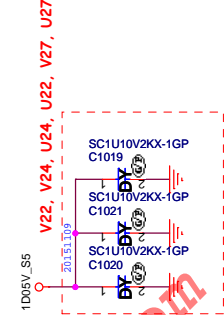
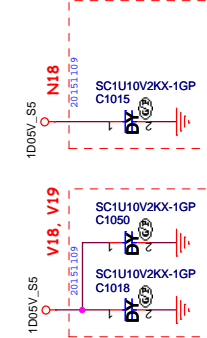
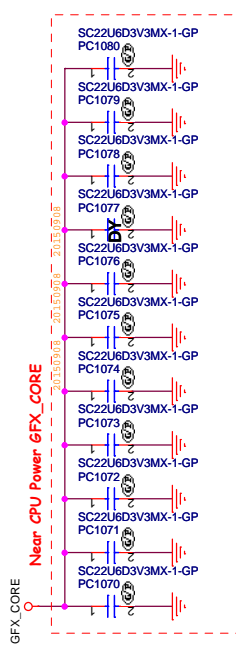
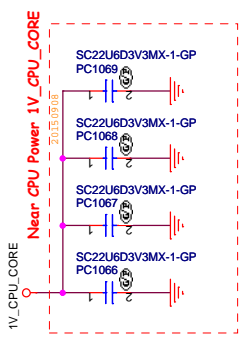
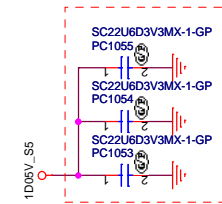
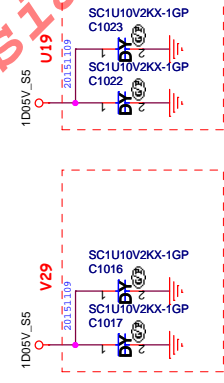
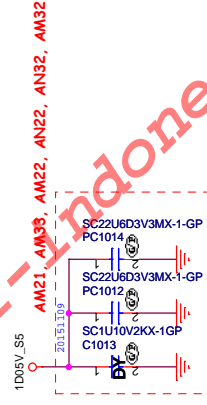
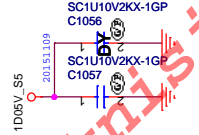
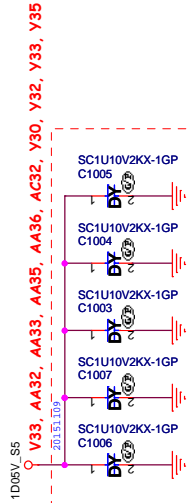
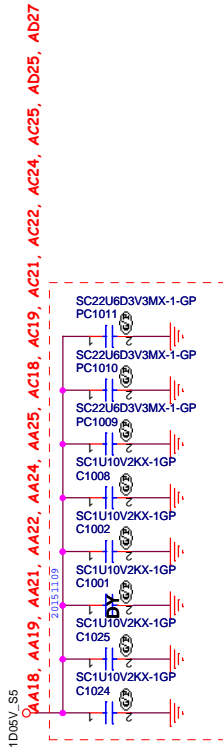
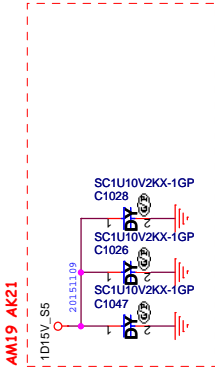
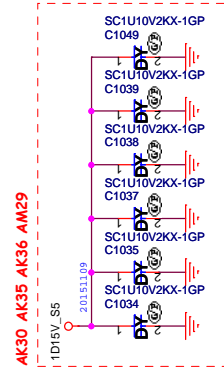
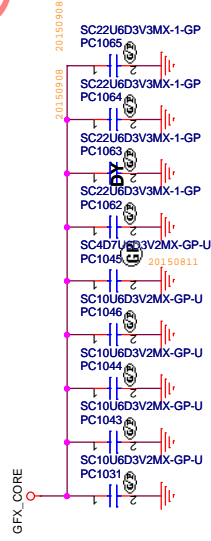
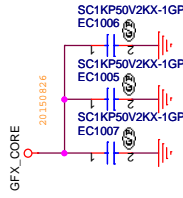
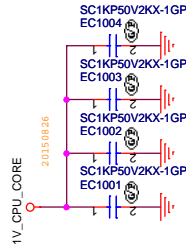
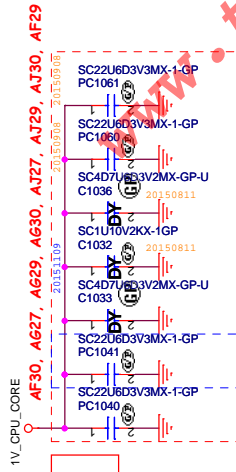
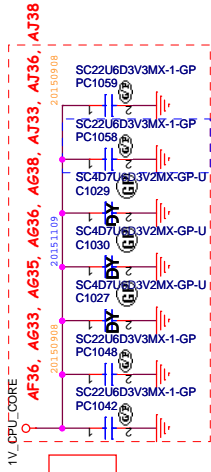
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CPU (VSS)			
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A3		X00	
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SSID = CPU

PLACE ALL THE CAPS
UNDER THE PKG SHADOW

PLACE ALL THE CAPS
UNDER THE PKG SHADOW



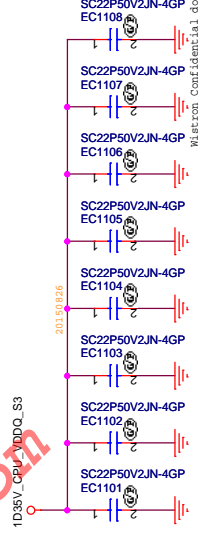
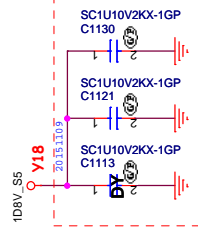
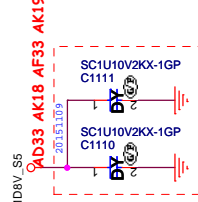
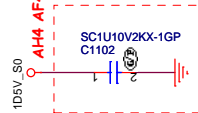
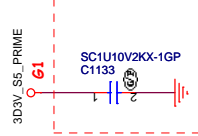
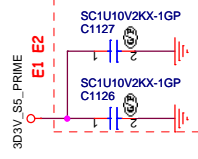
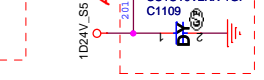
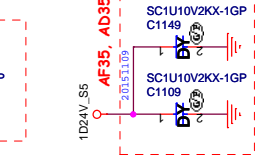
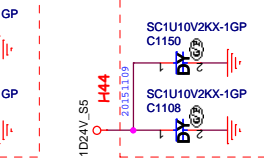
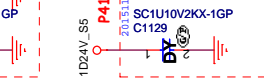
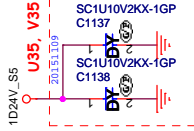
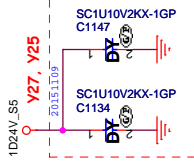
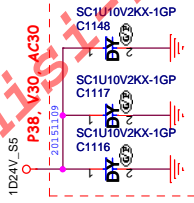
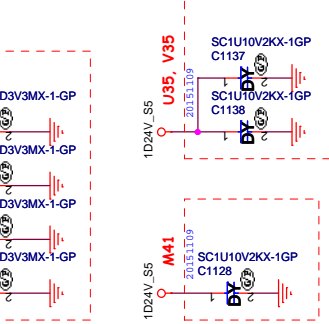
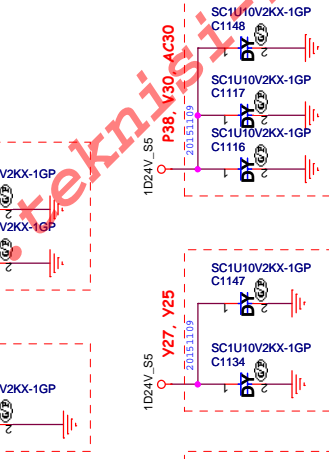
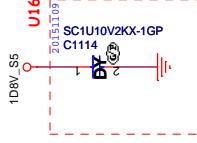
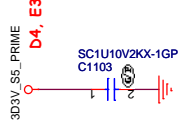
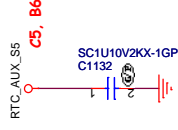
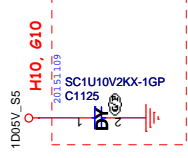
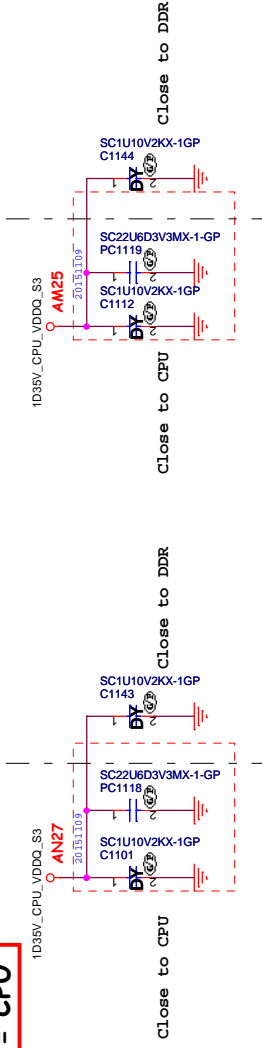
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File CPU (Power CAP1)

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SSID = CPU



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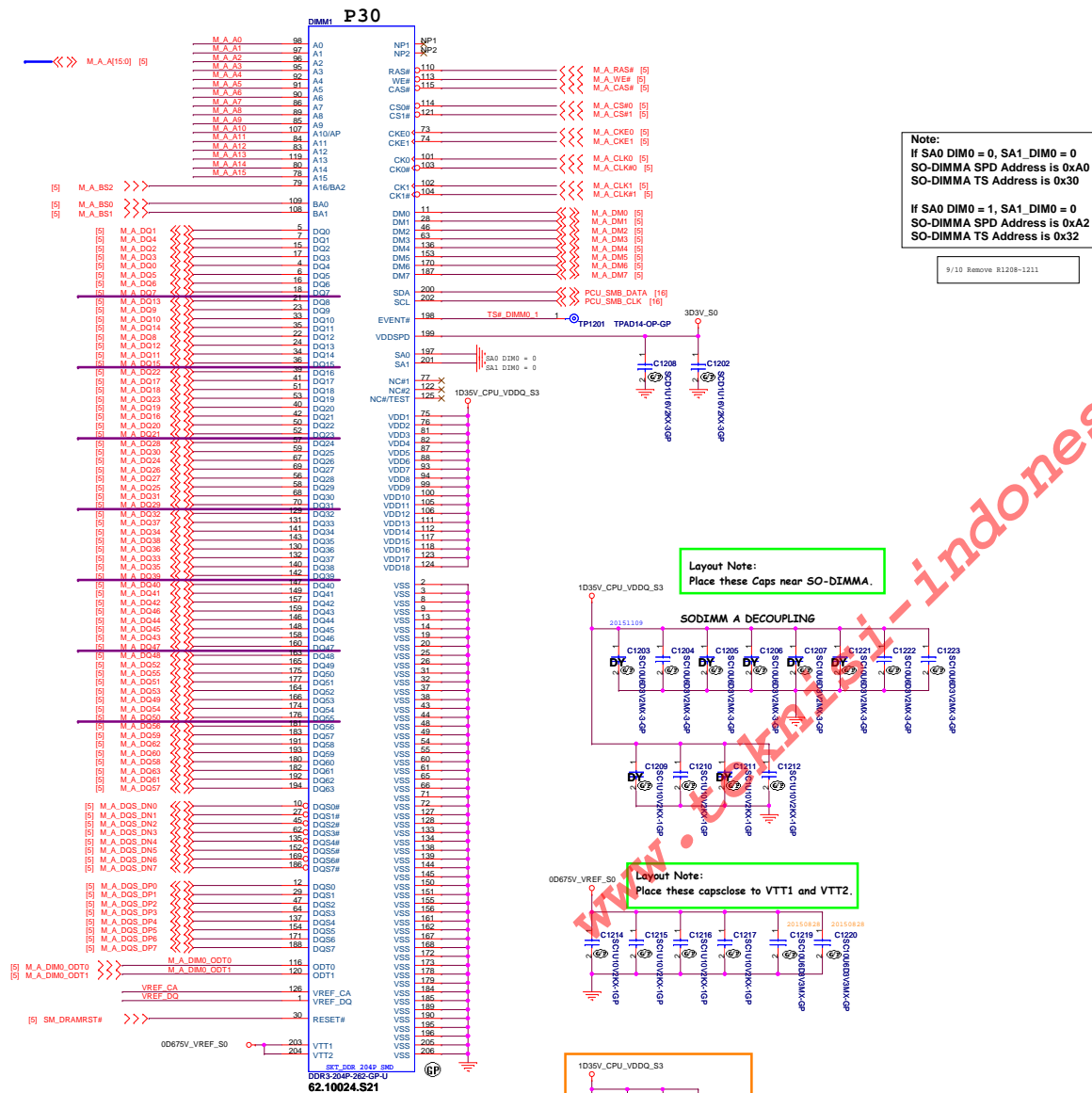
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CPU (Power CAP2)

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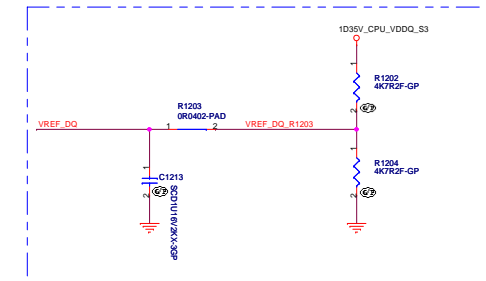
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

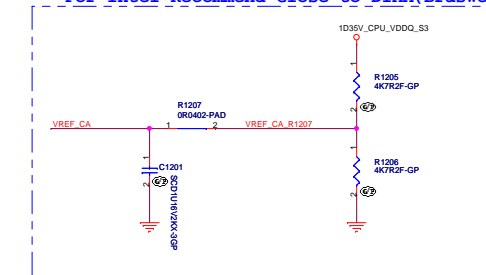
9/10 Remove R1208-1211

9/10 Remove RI201 (Thermal Event)

For Intel Recommend Close to DIMM(Braswell)

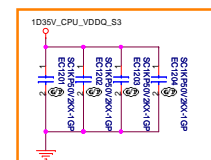


For Intel Recommend Close to DIMM(Braswell)



DD675V_VREF_S0

Layout Note:
Place these caps close to VTT1 and VTT2.




Reserve 0.1uF for ESD

SSID = MEMORY

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SSID = CPU

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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

All the straps are sampled on the rising edge of the
PMC_RSMRST_N signal (check list)

Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
GPIO	GPIO_SUS0	GPIO_SUS1	GPIO_SUS2	GPIO_SUS3	GPIO_SUS4	GPIO_SUS5	GPIO_SUS6	GPIO_SUS7	SEC_GPIO_SUS8	SEC_GPIO_SUS9	SEC_GPIO_SUS10	GP_CAMERA808	GP_CAMERA809	GP_CAMERA811
Schematic														
High	DDI0 Detect	DDI1 Detect	Normal Operation	DSI Detect	Boot from SPI	Weak internal pull-up Normal Operation	Normal	Weak internal pull-up Normal	1.35V	Weak internal pull-up Bypass with 1.05V	PMC	Bypass	Bypass	Bypass
Low	Disable	Disable	Change Boot Loader address (A16 Override)	Disable	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V	No bypass	Fuse controller	No bypass	No bypass	No bypass

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap override	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Strap Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

Table 29. Straps (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, ICLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERA808	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERA809	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERA811	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass


CHV Straps [CRB] -- strap detect @ RSMRST# assertion				
Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Weak)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	1- DDI0 Detect, 0- Disable	High
DDI1 Detected	GPIO_SUS1	PD	1- DDI1 Detect, 0- Disable	High
A16 swap override	GPIO_SUS2	PU	1- Default, 0- A16 override	High
DSI Display Detected	GPIO_SUS3	PD	1- DSI detect, 0- Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	1- Boot from SPI, 0- Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	1- Security enabled, 0- Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1- normal, 0- Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1- Normal, 0- Sus Debug enable	High
ICLK, USB2, DDI SFR Supply Select	SEC_GPIO_SUS8	PU	1- 1.35V, 0- 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	1- Bypass with 1.05V, 0- No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	1- PMC, 0- Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERA808	PD	1- Bypass, 0- No bypass	Low
CCU SUS RO Bypass	GP_CAMERA809	PD	1- Bypass, 0- No bypass	Low
RTC OSC Bypass	GP_CAMERA811	PD	1- Bypass, 0- No bypass	Low

SSID = CPU

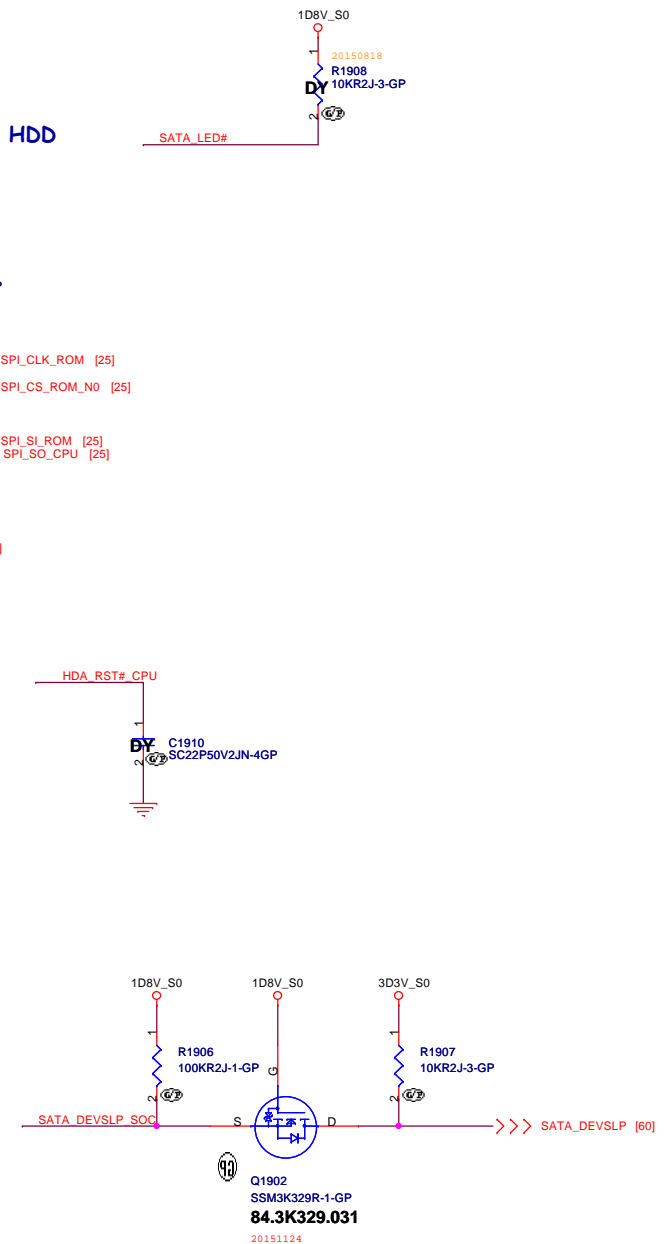
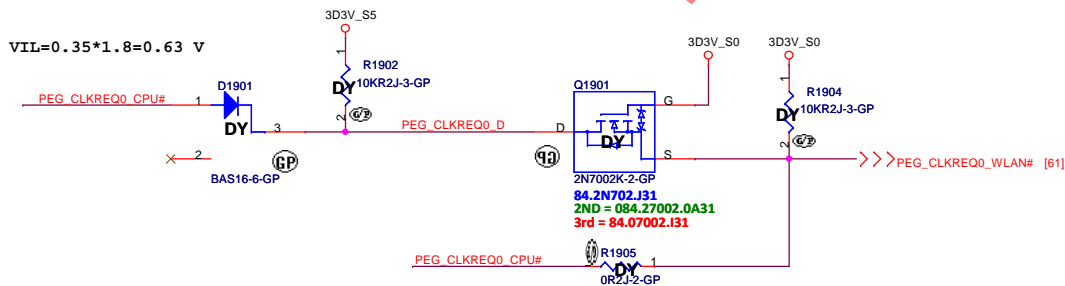
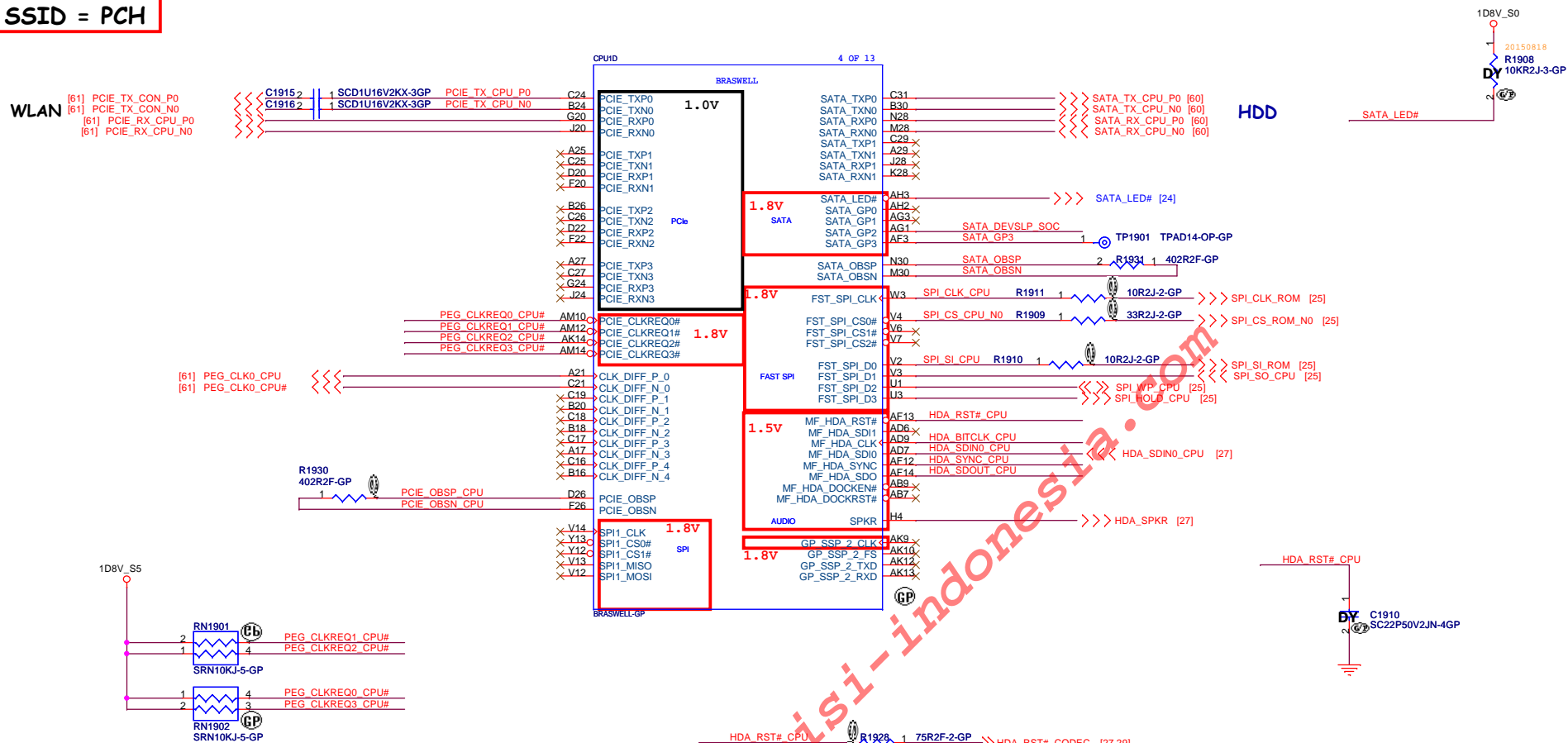
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Title (Reserved)			
Size A4	Document Number Rocket BSW 11.6"		Rev X00
Date: Monday, September 21, 2015		Sheet 17	of 109

SSID = PCH



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Title			
CPU (SATA/PCIE/IHDA)			
Size A3	Document Number		Rev
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Date:	Tuesday, November 24, 2015	Sheet 19 of	109


SSID = PCH

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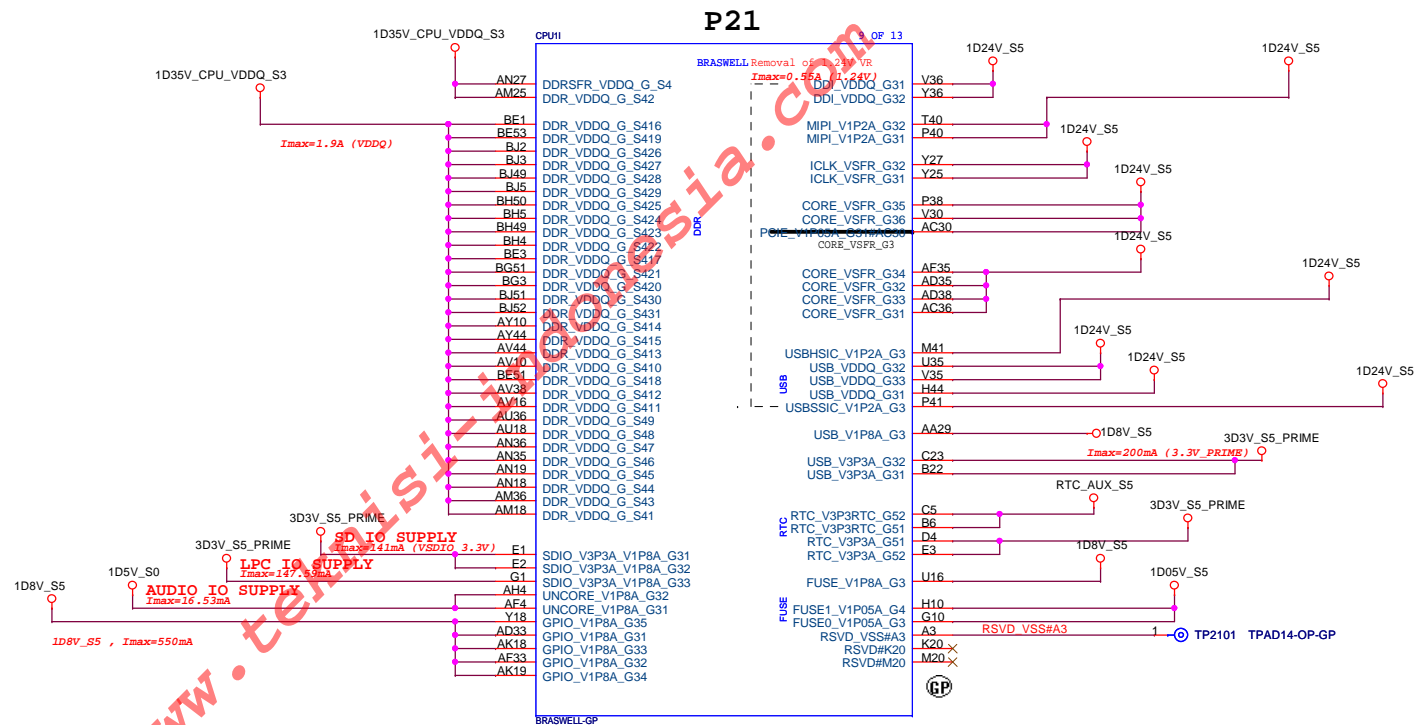
Title

(Reserved)

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Date: Monday, September 21, 2015	Sheet 20 of 109
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SSID = CPU



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Title

CPU (POWER1)Size
A3

Document Number

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Date: Monday, September 21, 2015

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Rev

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Date: Monday, September 21, 2015

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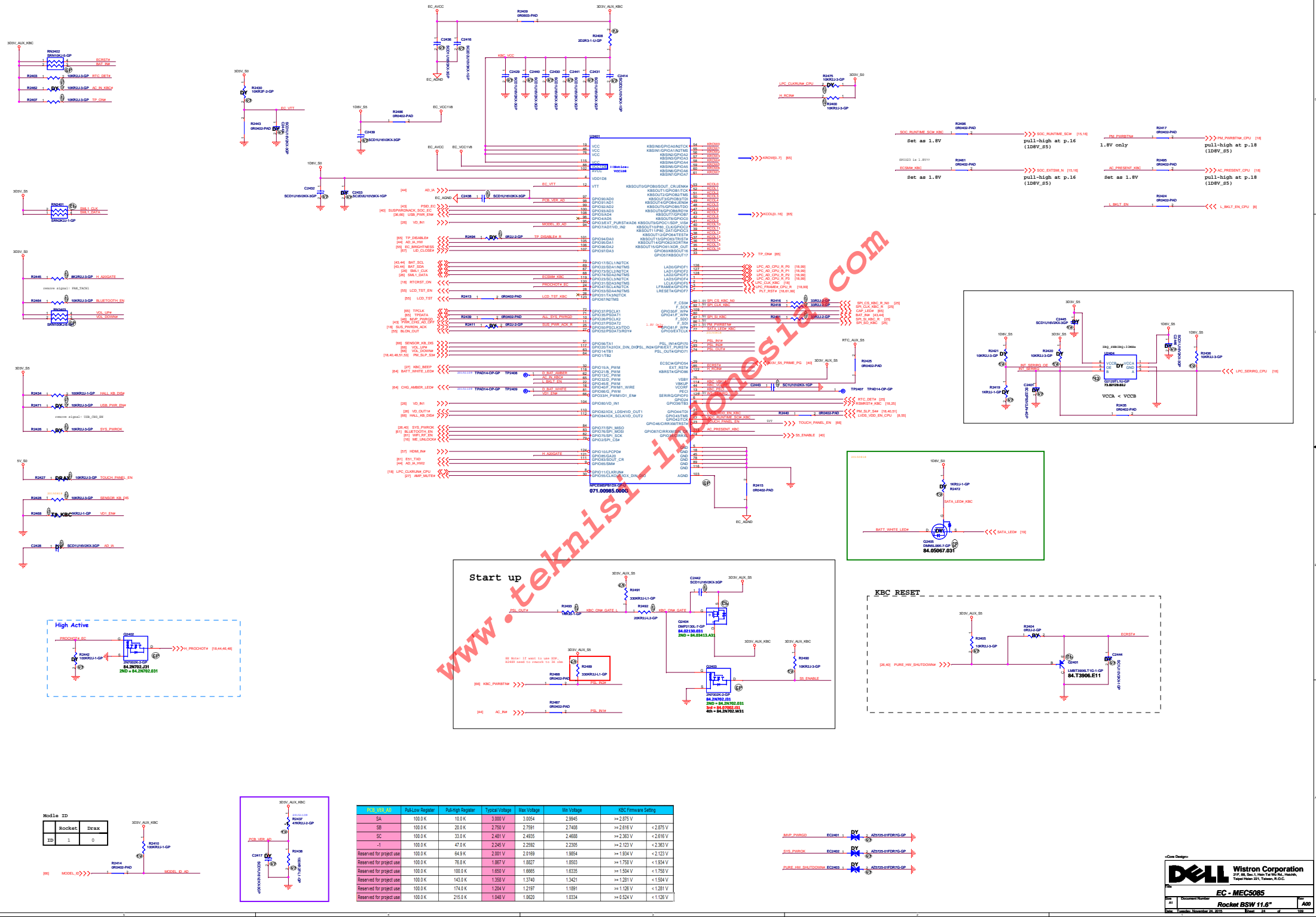
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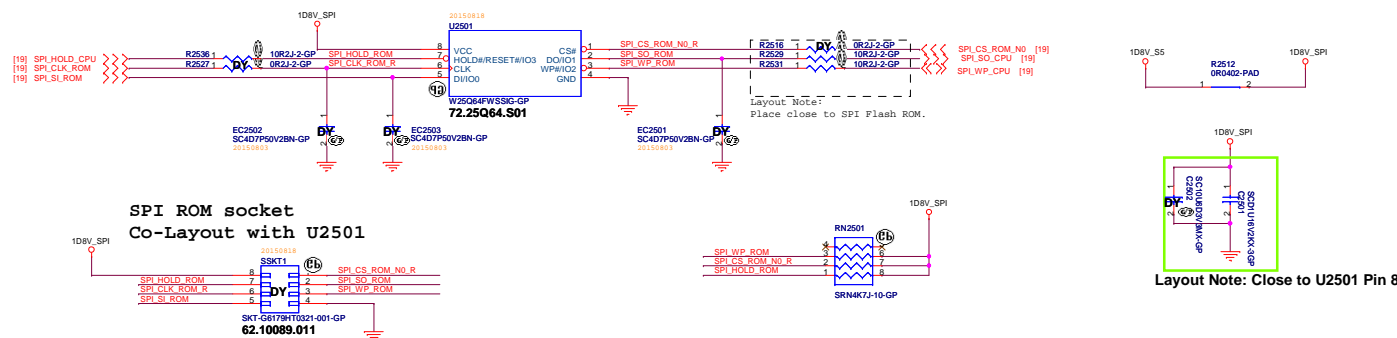
Title			(Reserved)		
Size	Document Number				Rev
A4	Rocket BSW 11.6"				X00
Date:	Monday, September 21, 2015			Sheet	23 of 109

SSID = KBC



SSID = Flash.ROM

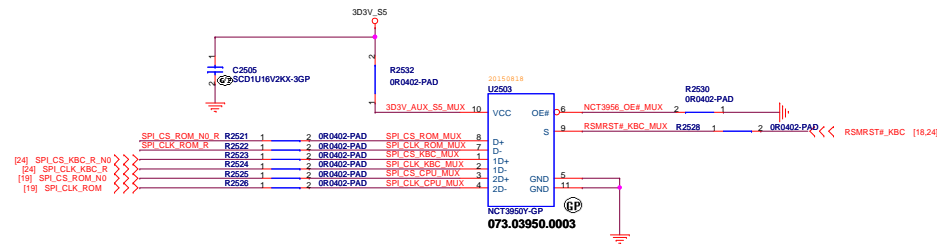
SPI FLASH ROM (8M byte) for CPU



SPI ROM link to KBC



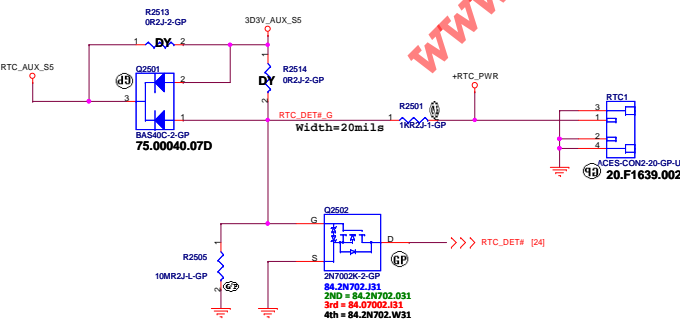
High Speed Switch for Share ROM



5240626:SPI Signals do not get tri-stated / MUX Sol.

Truth Table				
OE#	S	D+	D-	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	1D+	1D-	D=1D
L	H	2D+	2D-	D=2D

SSID = RTC

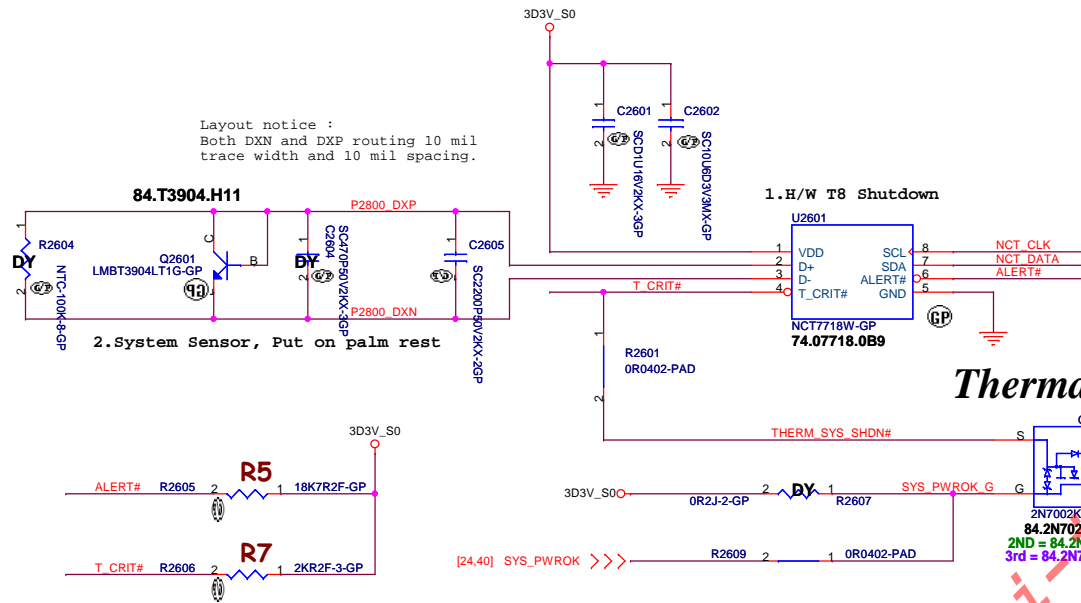


<Core Design>

SSID = Thermal

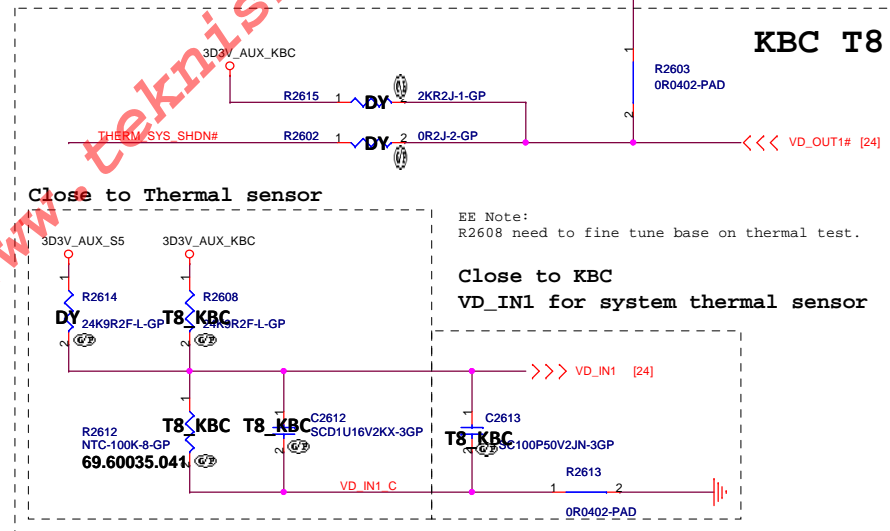
1. T8: PURE_HW_SHUTDOWN# through Q2603.
2. THM_SENSOR: Thermal sensor NCT7718W solution.

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

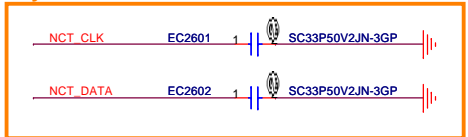


The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



Layout Note: Close U2601



pull-high at p.24
(3D3V_S5)

—<> SML1_DATA [24]

Thermal sensor NCT 7718W

KBC T8

EE Note:
R2608 need to fine tune base on thermal test.

Close to KBC
VD_IN1 for system thermal sensor

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Title			
<i>Thermal</i>			
Size A3	Document Number <i>Rocket BSW 11.6"</i>		Rev <i>X00</i>
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Size
A4

Document Number

Rocket BSW 11.6"

Rev
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Date: Monday, September 21, 2015

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SSID = LOM

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Size
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Date: Monday, September 21, 2015


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SSID = LAN

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Title (Reserved)LAN			
Size A4	Document Number Rocket BSW 11.6"		Rev X00
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SSID = LAN CONN

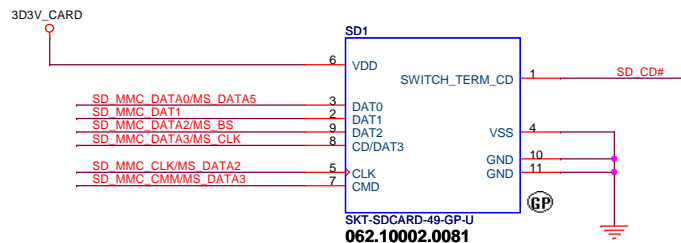
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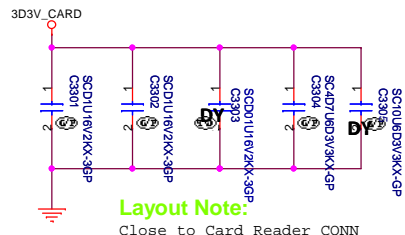
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)RJ45+Transformer		
Size A4	Document Number Rocket BSW 11.6"	Rev X00
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SSID = Card Reader

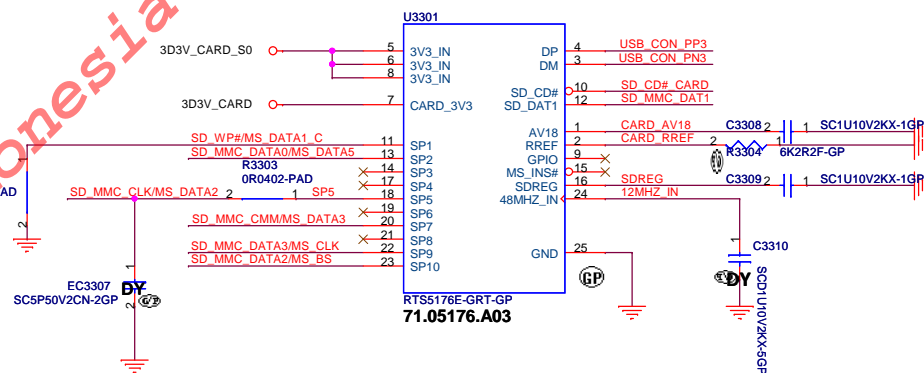
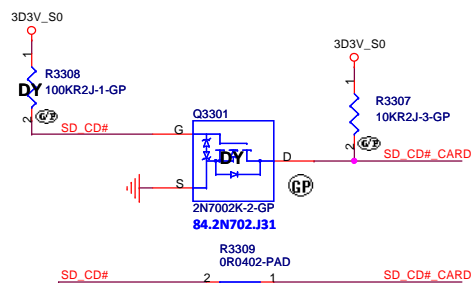


SD Card Connector

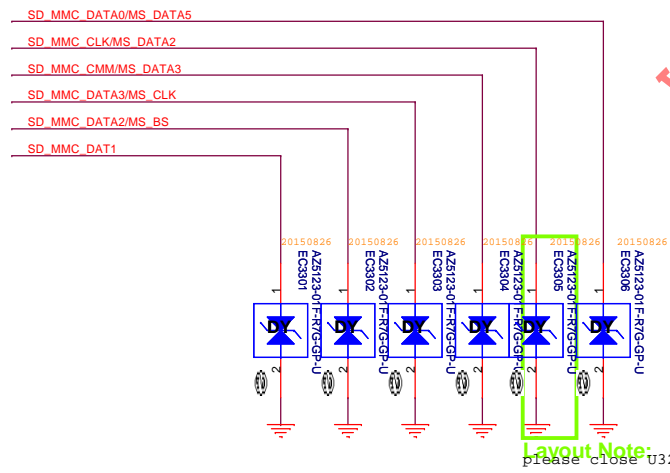
Pin	Define
P1	SWITCH TERM CD
P2	DAT1
P3	DAT0
P4	VSS
P5	CLK
P6	VDD
P7	CMD
P8	CD/DAT3
P9	DAT2
P10	GND
P11	GND



Layout Note:
Close to Card Reader CONN

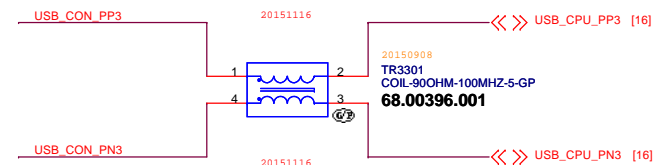


For EMI Reserved



Layout Note:
please close U3201

Pin name	Net name
SD_DAT1	SD_MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD_MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD_MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD_MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD_MMC_DATA3/MS_CLK
SP10	SD_MMC_DATA2/MS_BS



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Title Card Reader + CONN		
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Date: Tuesday, November 17, 2015	Sheet 33	of 109

SSID = USB

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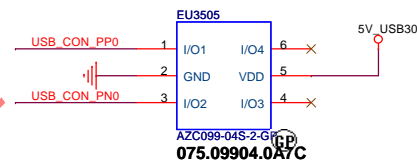
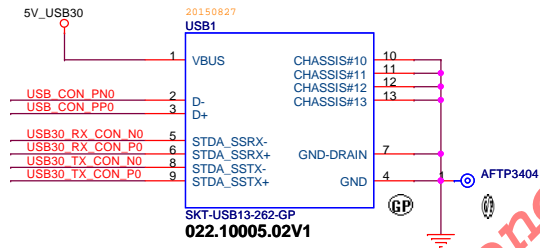
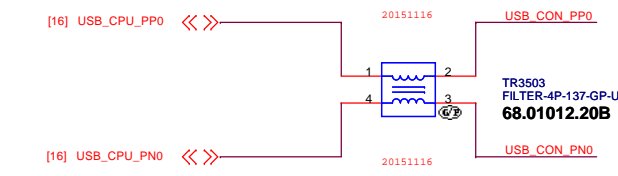
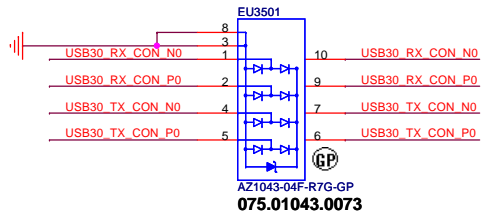
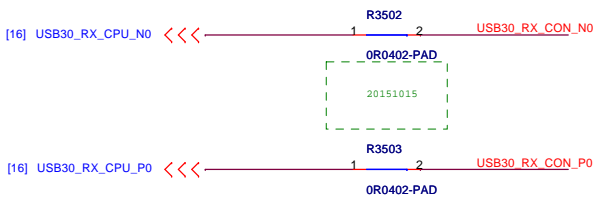
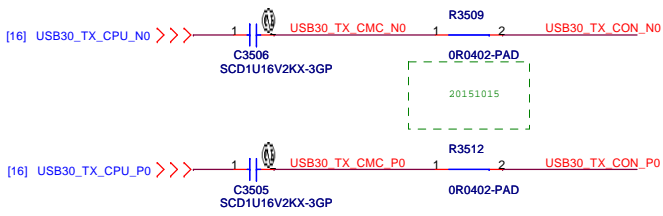
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Title
(Reserved)USB 2.0 Port

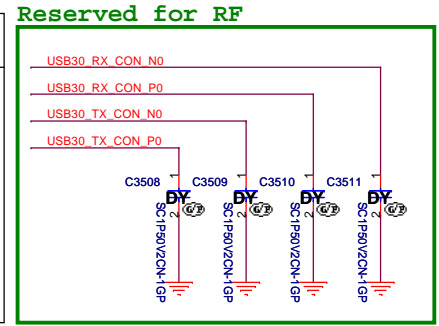
Size A4	Document Number Rocket BSW 11.6"	Rev X00
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Date: Monday, September 21, 2015 Sheet 34 of 109

SSID = USB

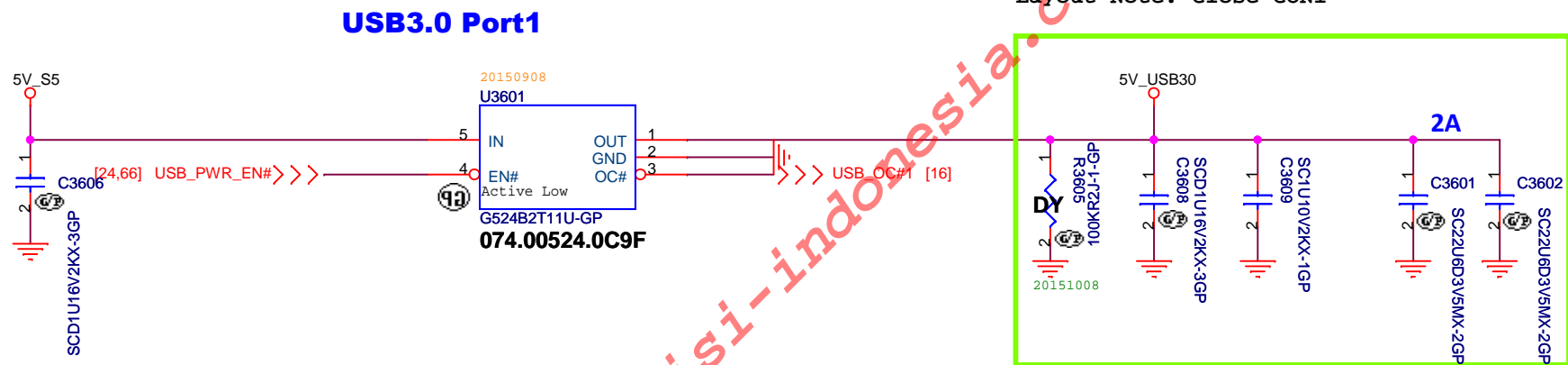


USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



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Reserved for RF



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Title

USB Power SW

Size
A4

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Date: Thursday, October 08, 2015

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SSID = USB

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Title

USB2.0 HUB

Size
A4

Document Number

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Date: Monday, September 21, 2015

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A4

Document Number

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Power Sequence



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Size
A4

Document Number

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X00

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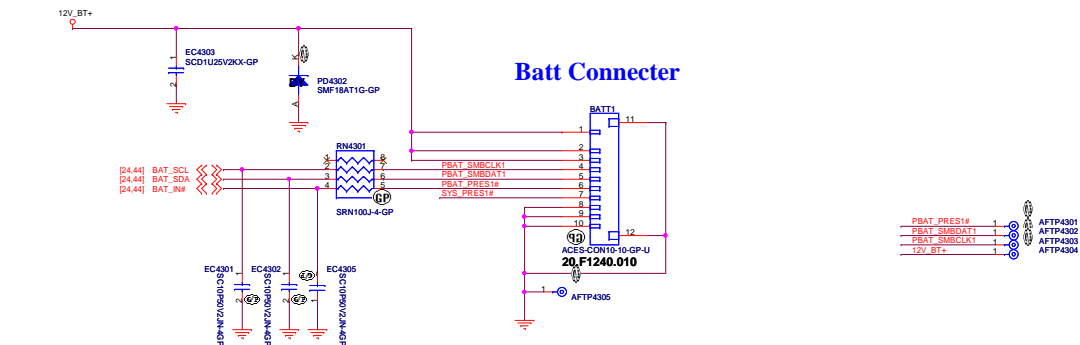
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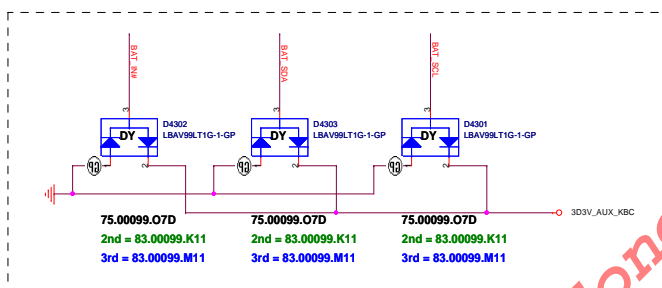
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Title			(Reserved)		
Size	Document Number				Rev
A4	Rocket BSW 11.6"				X00
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```
SSID = PWR.Support
```



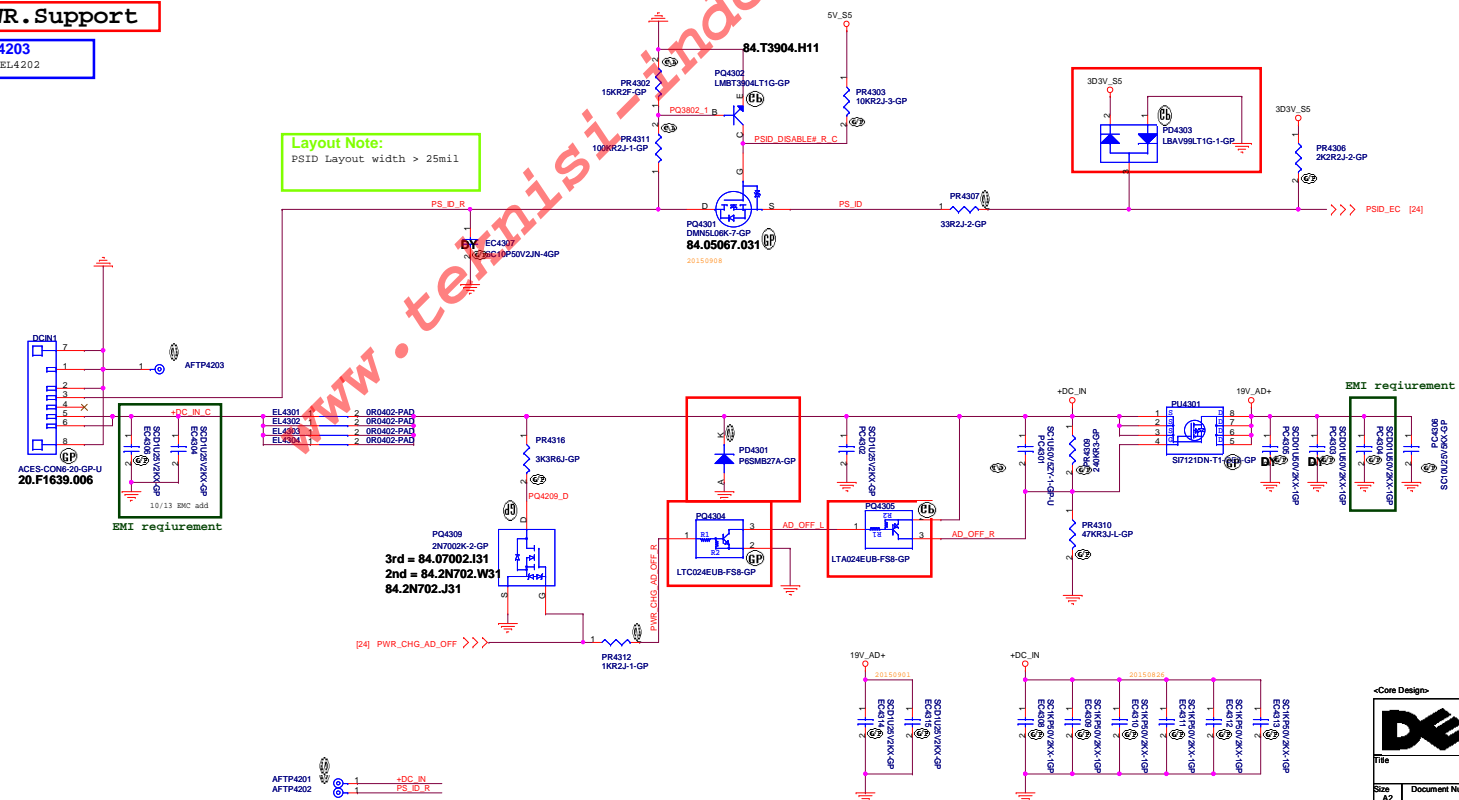
Placement: Close to Batt Connector



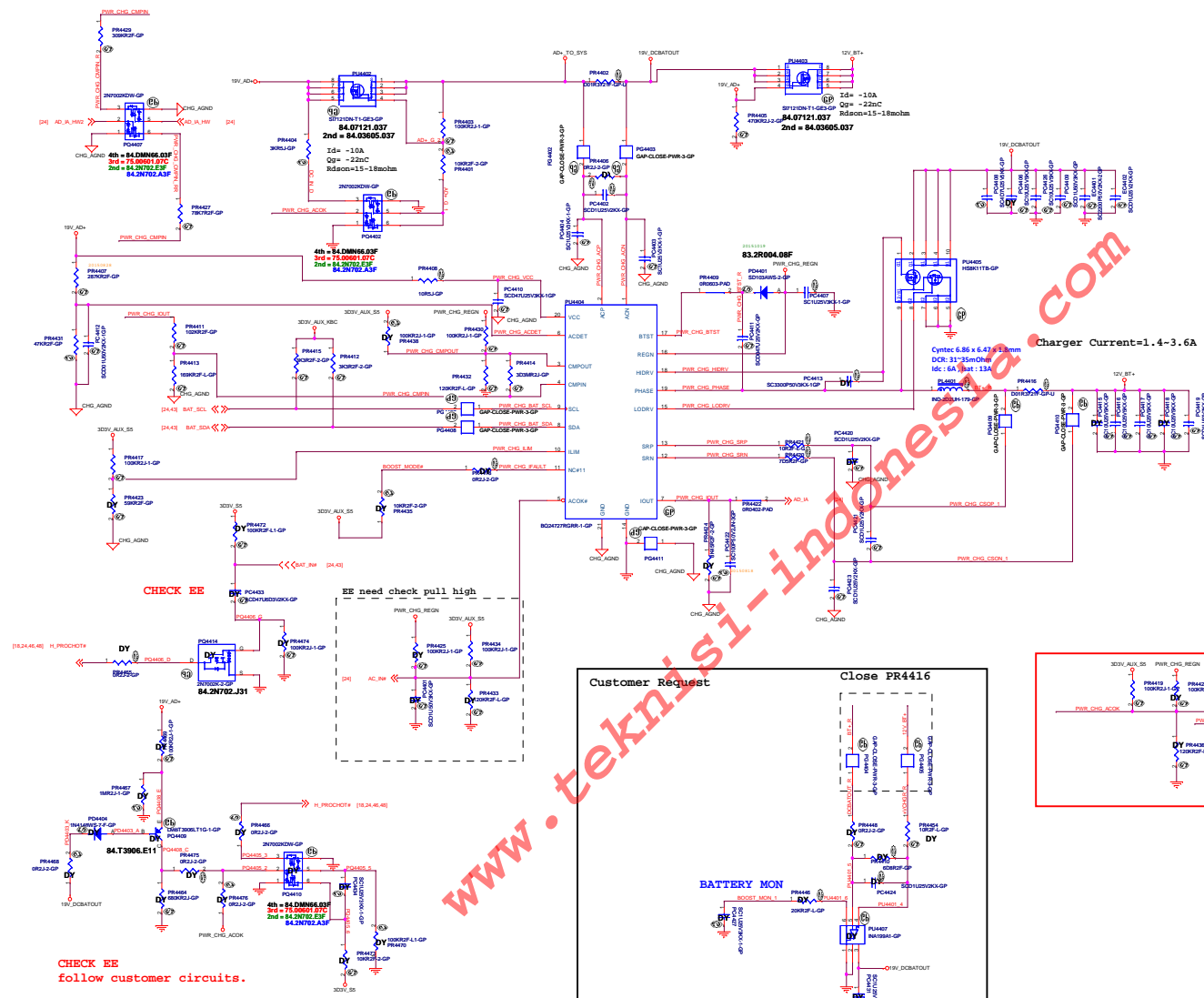
```
SSID = PWR.Support
```

0103 Add EC4203

Layout Note:
PSID Layout width > 25mil



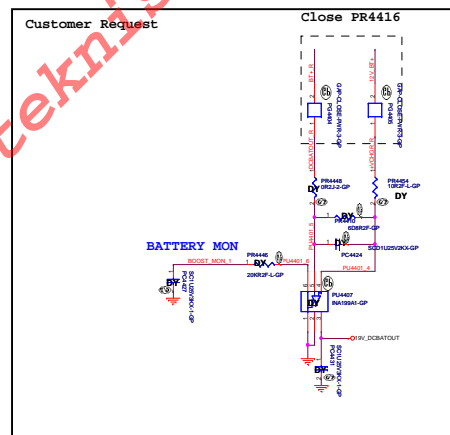
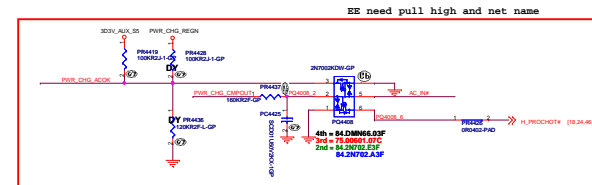
Main Func = Charger

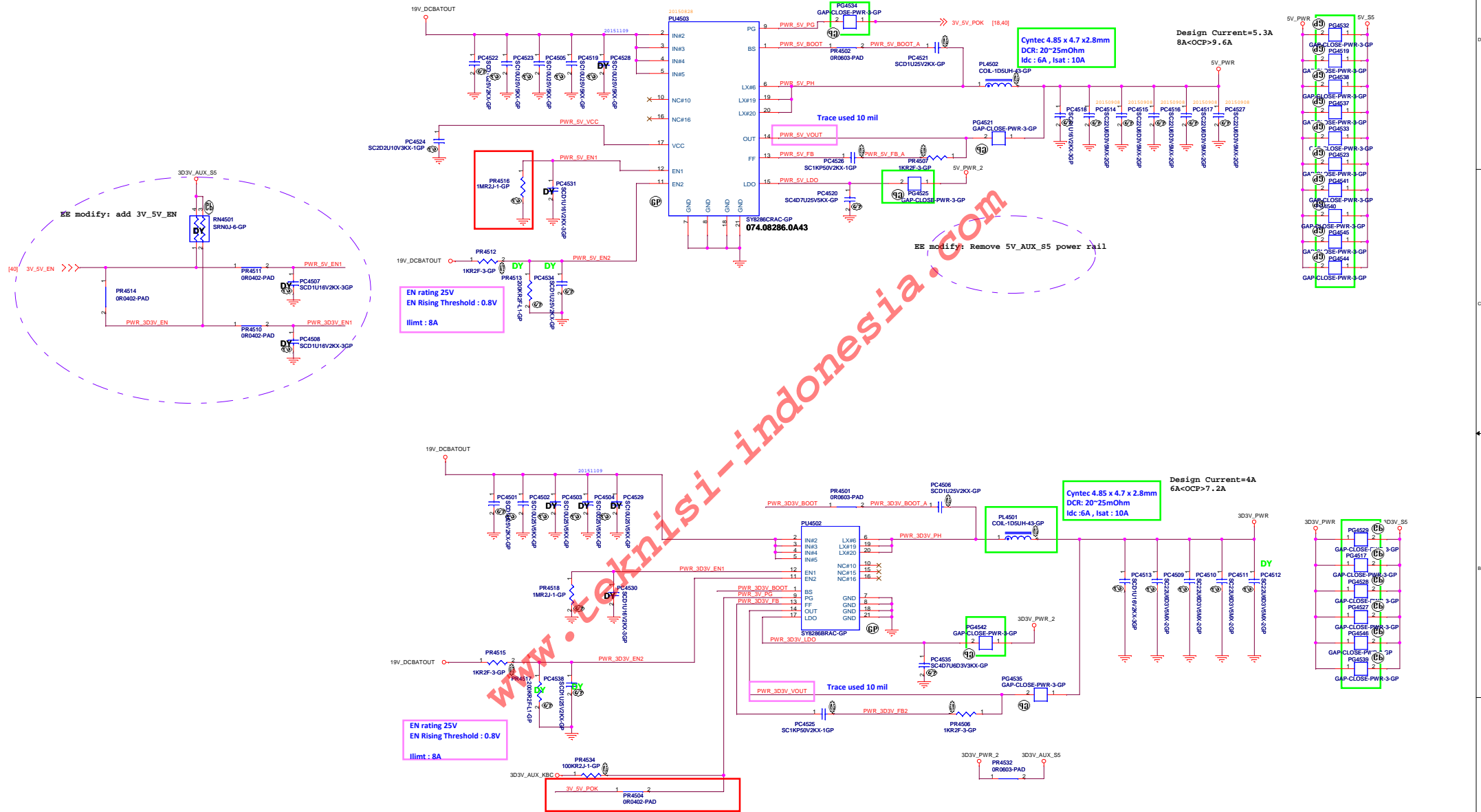


EC code only BQ24727

H_PROCHOT#	AD_IA_HW	AD_IA_
35W	0	0
45W	1	0
65W	0	1

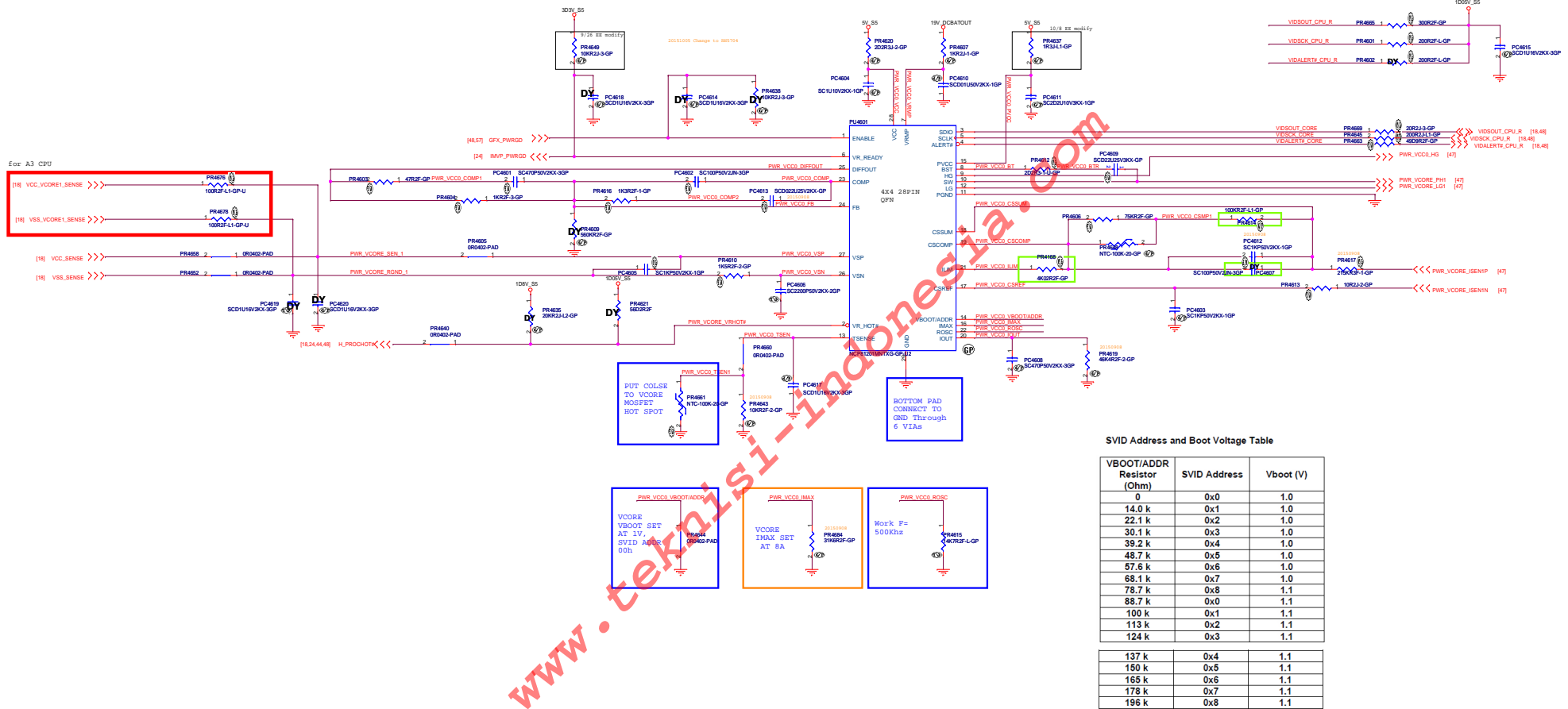
Center 6.86 x 6.47 x 1.8mm Charger Current=1.4~3.6A



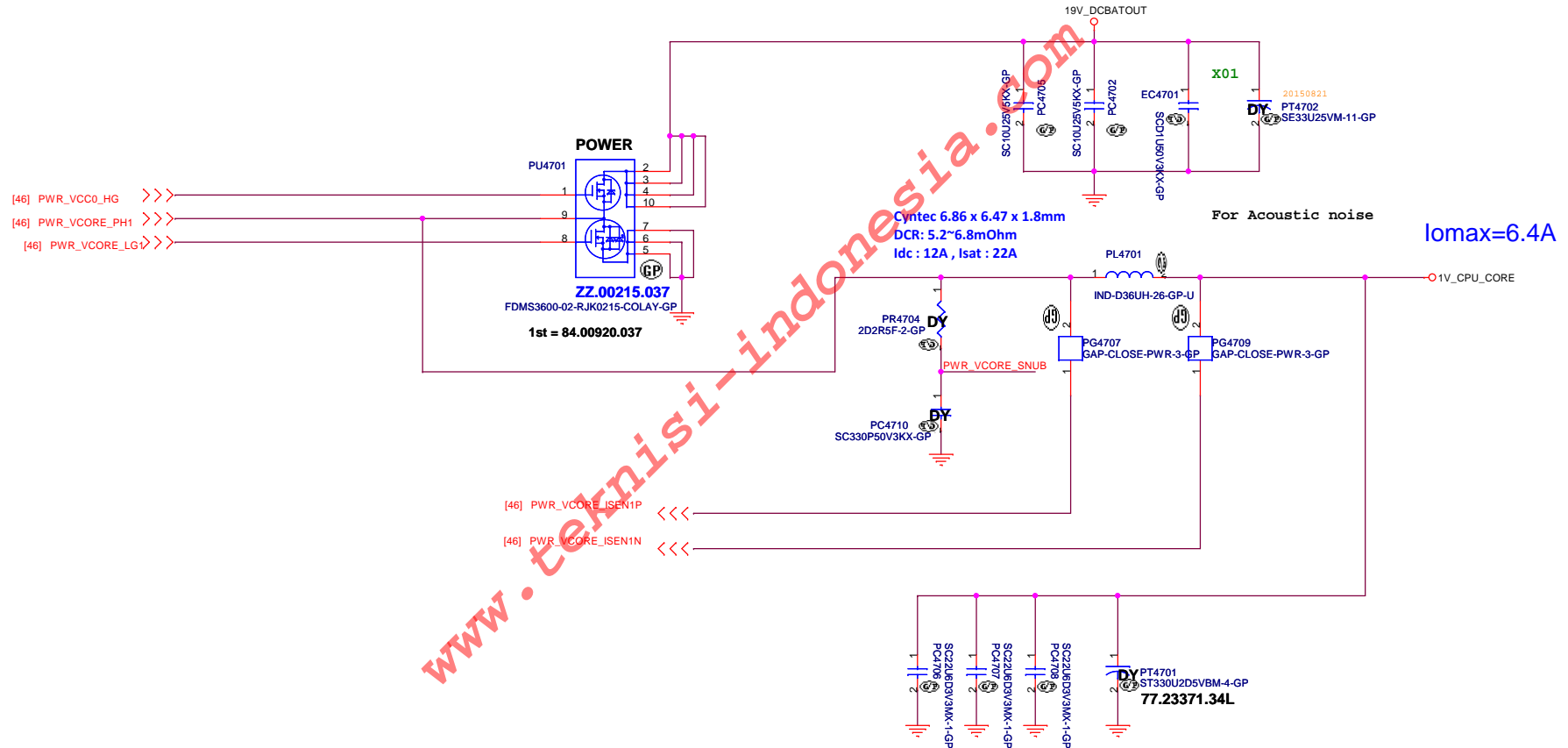


<Core Design>

SSID = CPU Regulator

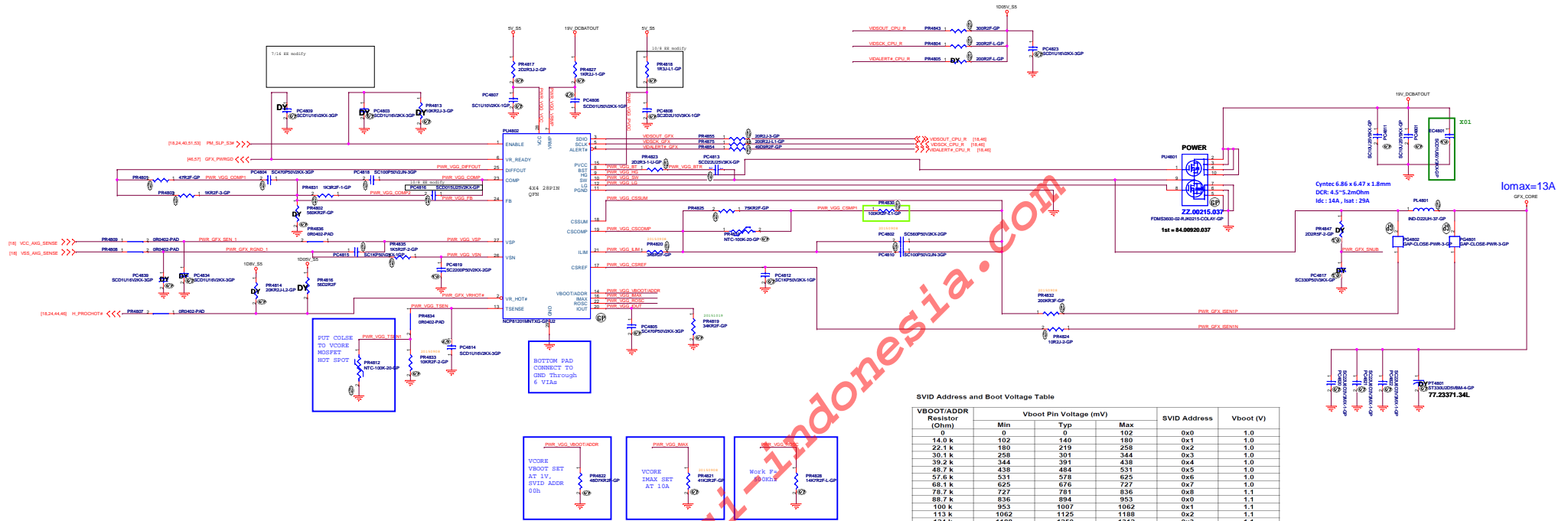


SSID = CPU Regulator



<Core Design>

SSID = GFX Regulator



SVID Address and Boot Voltage Table

VBOOT/ADDR	Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max			
0	0	0	102	0x0	1.0	
14.0 k	102	180	140	0x1	1.0	
22.1 k	180	219	258	0x2	1.0	
35.1 k	258	344	344	0x3	1.0	
39.2 k	344	391	430	0x4	1.0	
48.7 k	438	484	531	0x5	1.0	
53.7 k	531	578	625	0x6	1.0	
68.1 k	625	676	727	0x7	1.0	
72.7 k	727	781	836	0x8	1.1	
88.7 k	836	894	953	0x9	1.1	
100 k	953	1062	1125	0xA	1.1	
113 k	1062	1125	1188	0xB	1.1	
124 k	1188	1251	1312	0xC	1.1	
137 k	1312	1378	1445	0xD	1.1	
150 k	1445	1511	1578	0xE	1.1	
163 k	1578	1644	1719	0xF	1.1	
178 k	1719	1789	1859	0x10	1.1	
186 k	1859					

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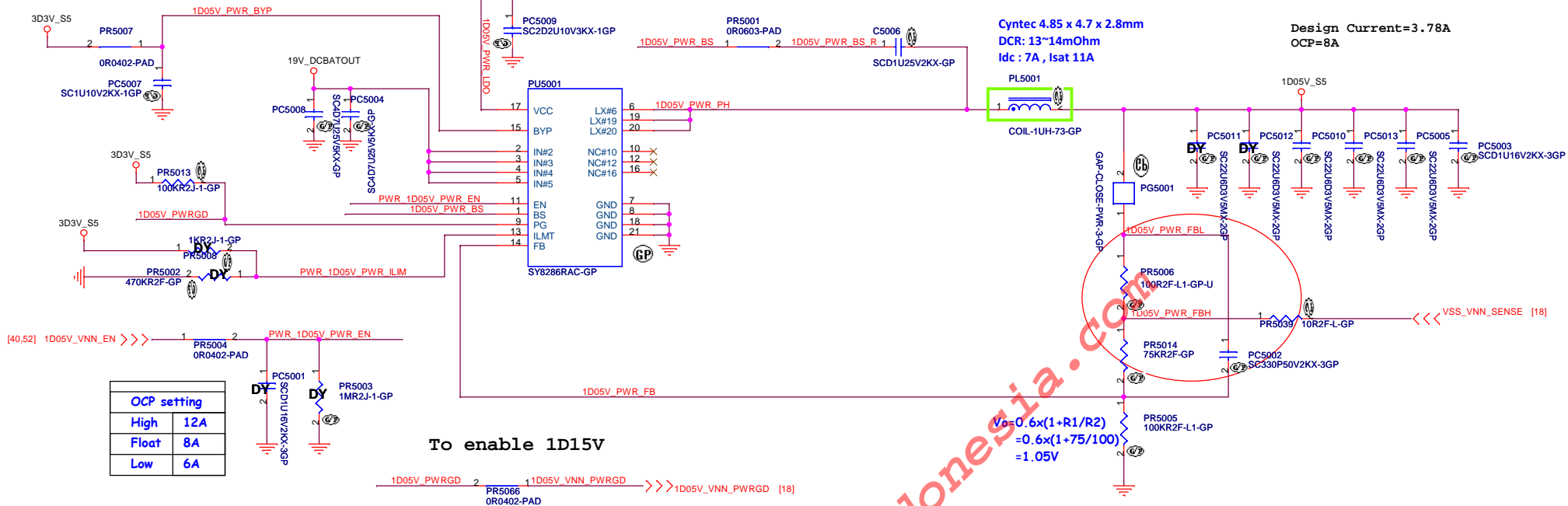
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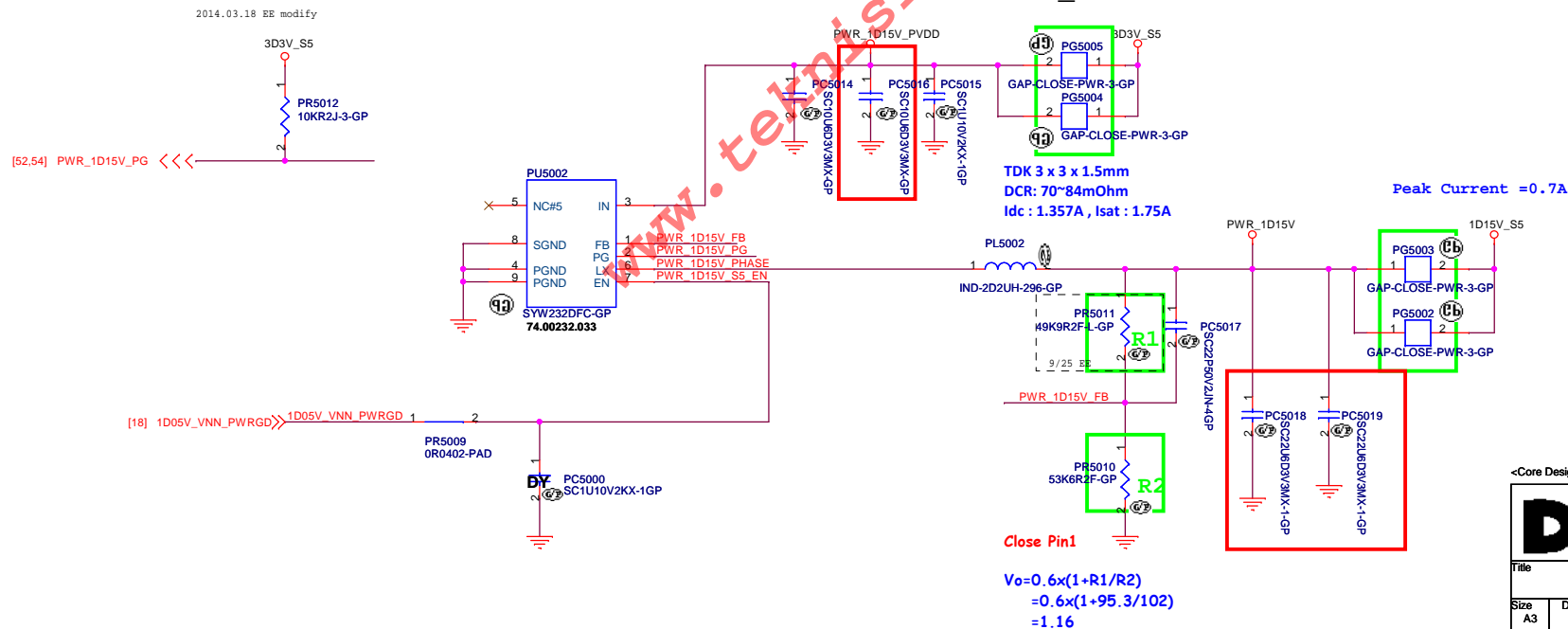
Title			(Reserved)		
Size	Document Number				Rev
A4	Rocket BSW 11.6"				X00
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SY8286D for 1D05V



```
SSID = PWR.Plane.Regulator_1p8v
```

SYW232 for 1D15V_S5



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Title

DCDC VNN 1D05V 1D15V

Size
A

Document Number

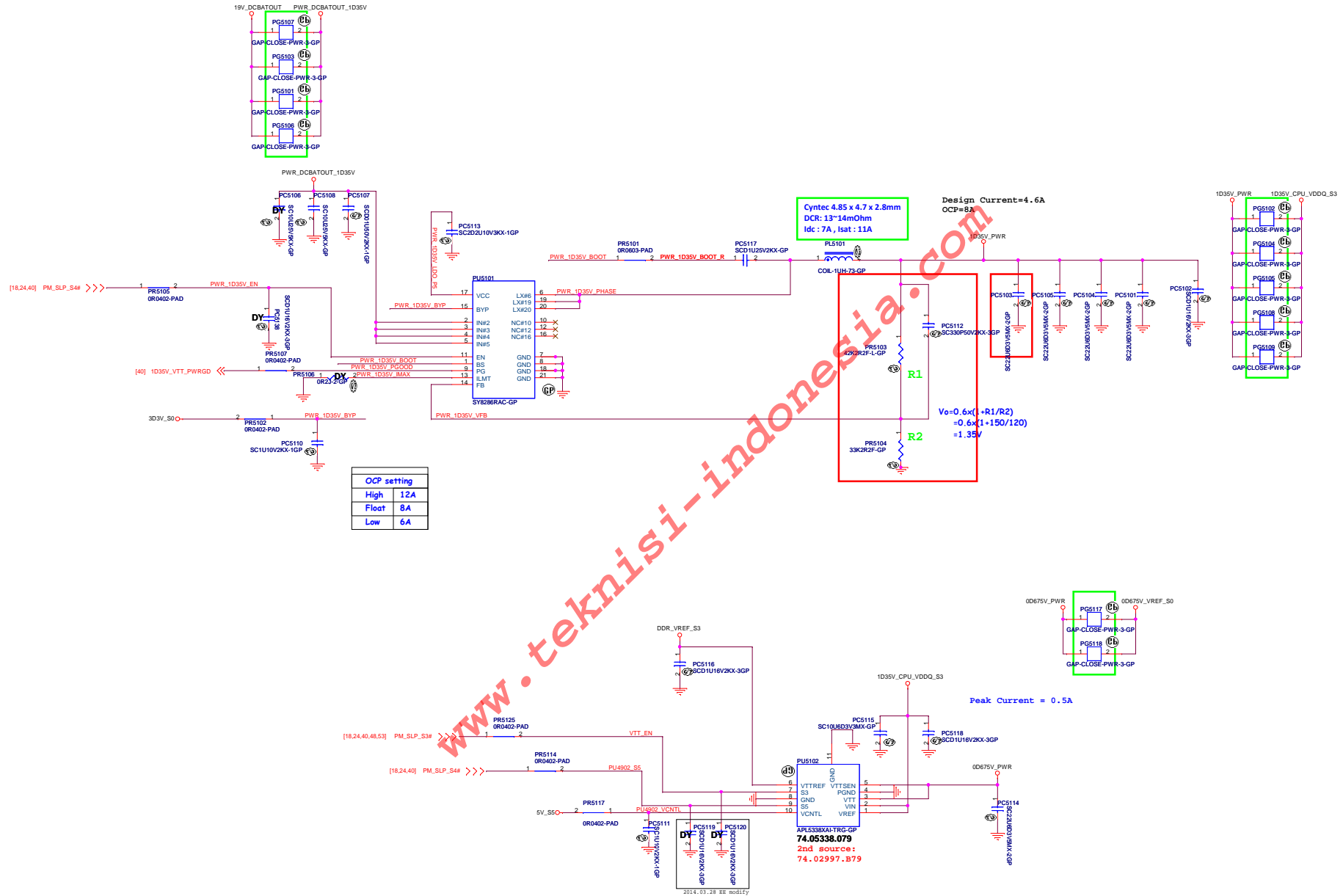
Rocket BSW 11.6"

Rev	X00
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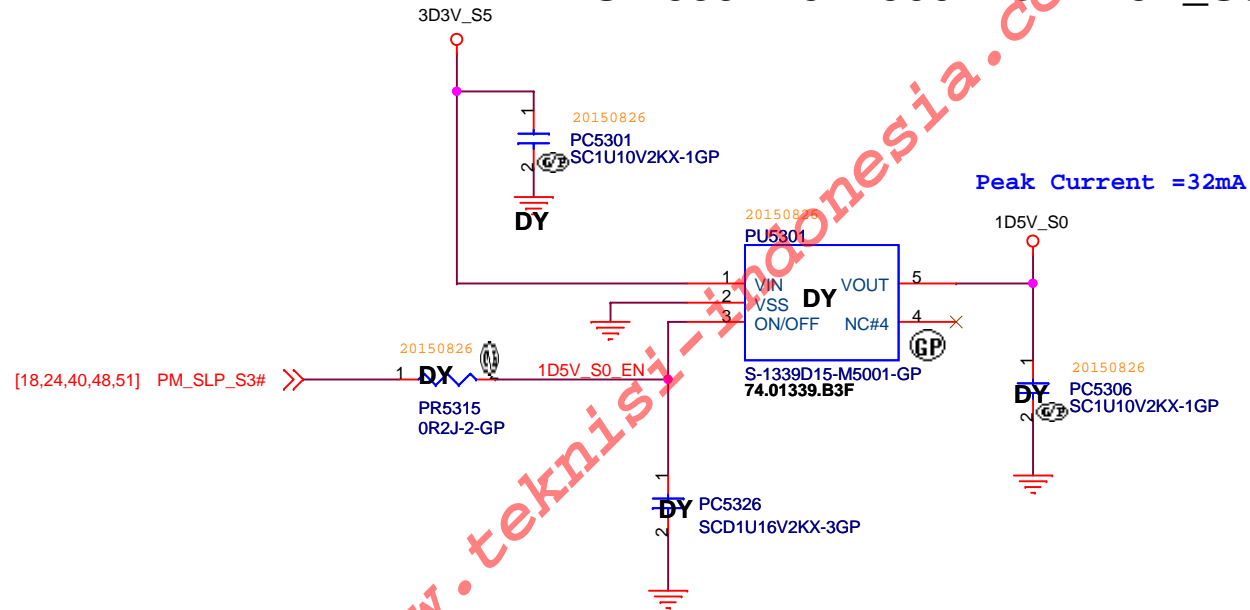
Date: Tuesday, October 06, 2015

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SY8206D for 1D35V



S-1339D15-M5001 for 1D5V_S0



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Title

S1339D15 1D5V

Size
A4

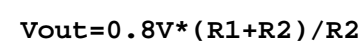
Document Number

Rocket BSW 11.6"

Rev
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Date: Tuesday, October 06, 2015

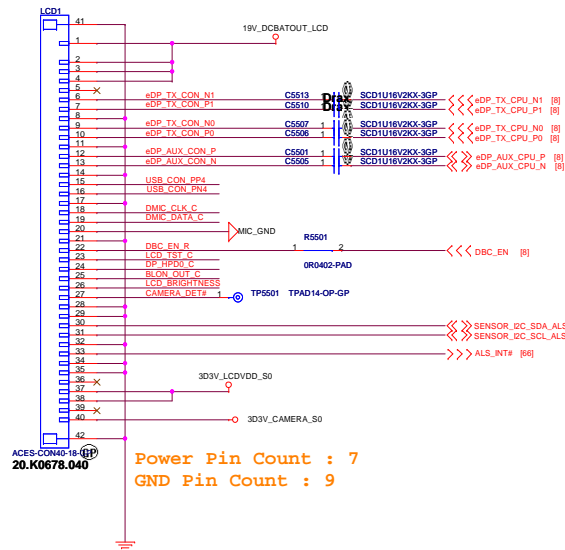
Sheet 53 of 109

[illegible]

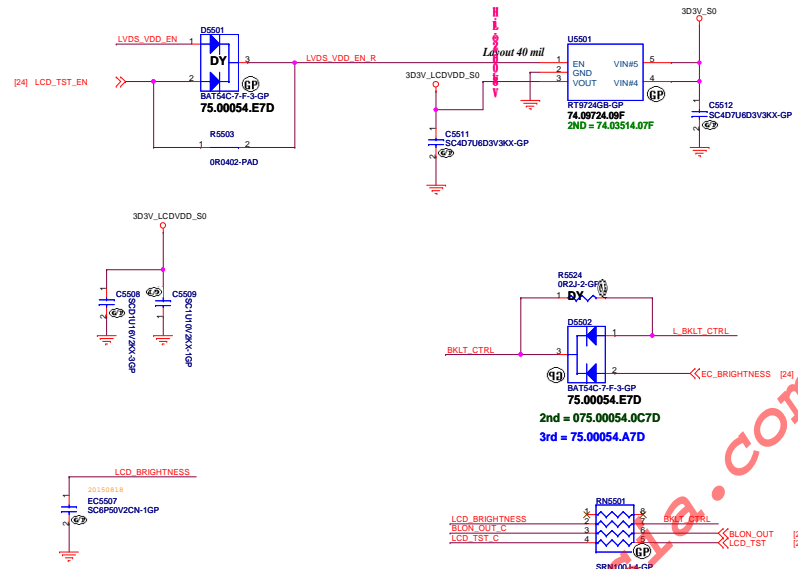
Title			
APL5930_1D24V			
Size A3	Document Number	Rocket BSW 11.6"	Rev A00
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SSID = VIDEO

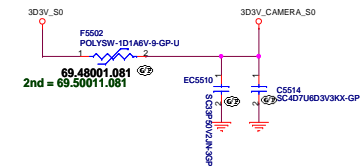
Panel Conn.



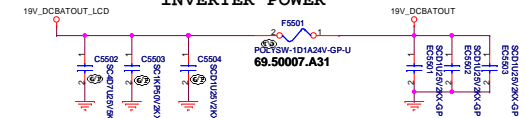
```
Power Pin Count : 7
GND Pin Count : 9
```



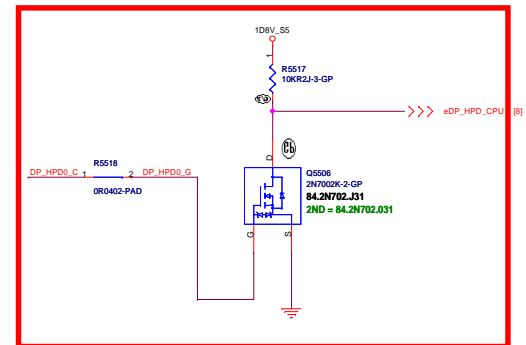
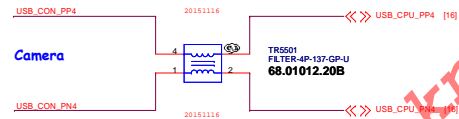
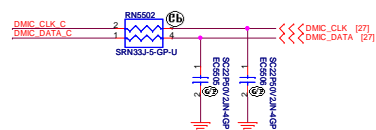
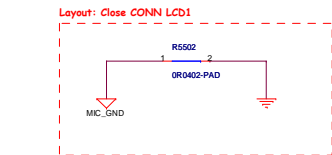
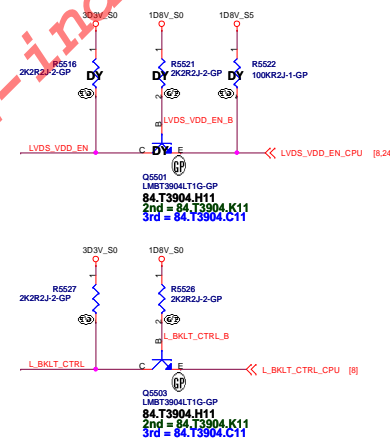
CAMERA POWER



INVERTER POWER



Level shift



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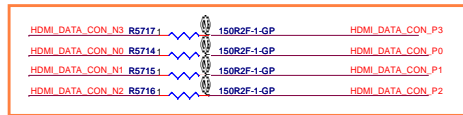
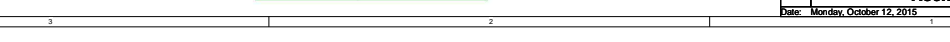
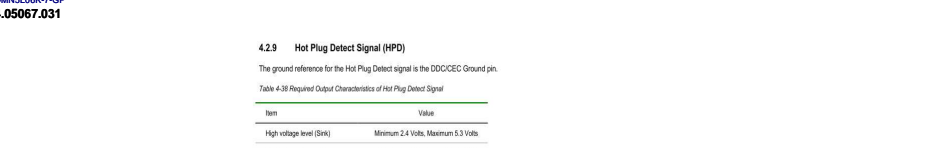
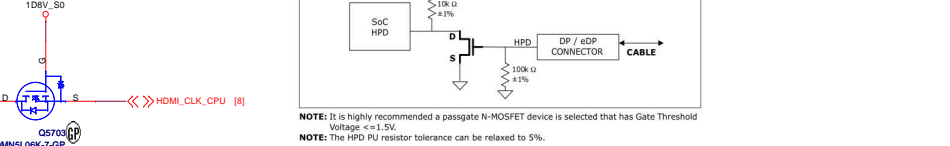
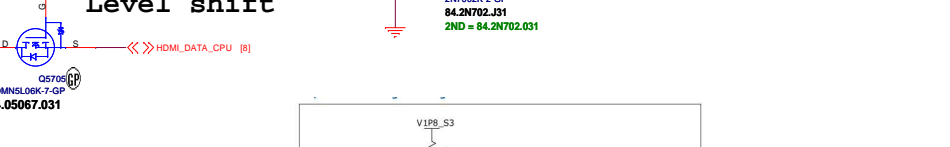
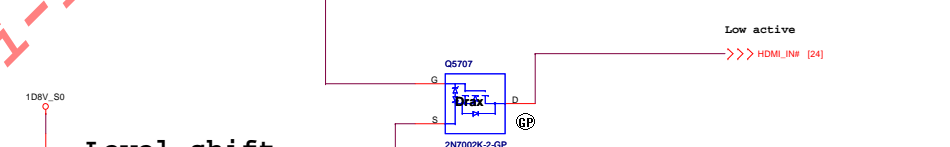
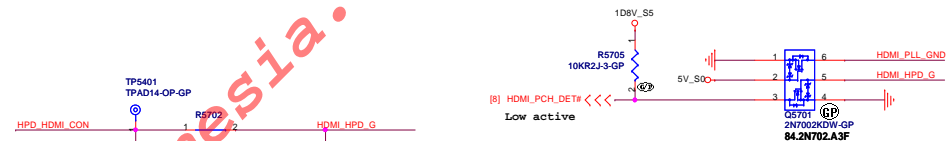
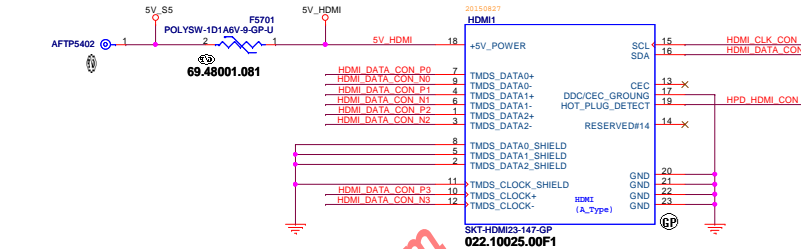
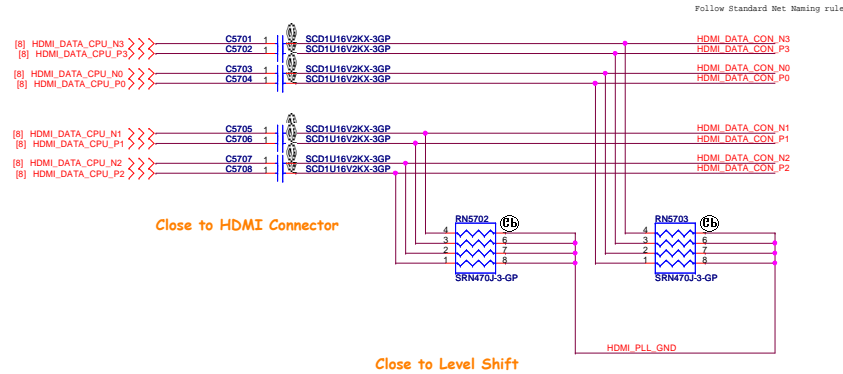
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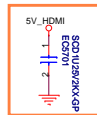
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HDMI Level Shifter & CONNECTOR



Reserve 150 ohm bridge resistance on the HDMI trace as circle for EMI



Reserve 0.1uF for ESD

4.2.9 Hot Plug Detect Signal (HPD)

The ground reference for the Hot Plug Detect signal is the DDC/CEC Ground pin.

Table 4-38 Required Output Characteristics of Hot Plug Detect Signal

Item	Value
High voltage level (Sink)	Minimum 2.4 Volts, Maximum 5.3 Volts
Low voltage level (Sink)	Minimum 0 Volts, Maximum 0.4 Volts
Output resistance	1000 ohms ±20%

Table 4-39 Required Detection Levels for Hot Plug Detect Signal

Item	Value
High voltage level (Source)	Minimum 2.0 Volts, Maximum 5.3 Volts
Low voltage level (Source)	Minimum 0 Volts, Maximum 0.8 Volts


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SSID = Display Port

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SSID = DVI

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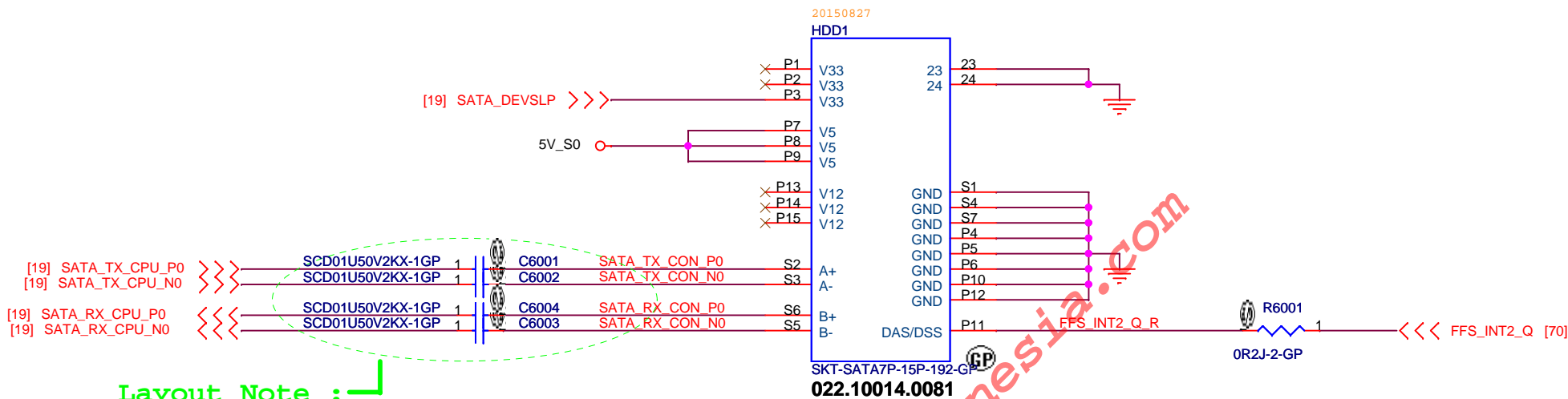
Title (Reserved) DVI

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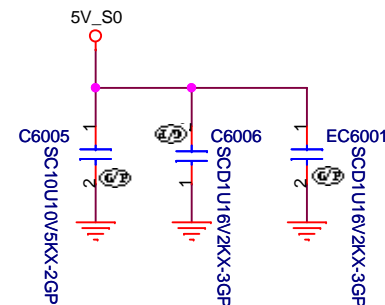
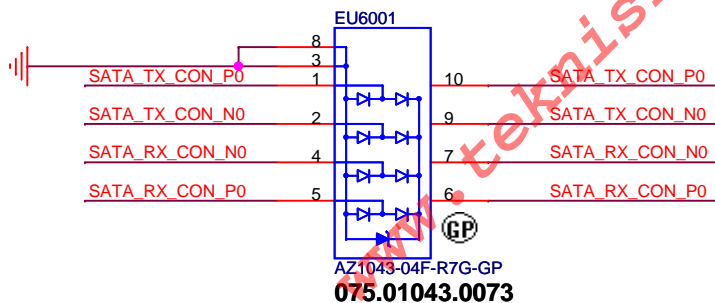
SSID = SATA

SATA HDD Connector



Layout Note :

AC coupling Cap;
place near CONN(<100mils)



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HDD

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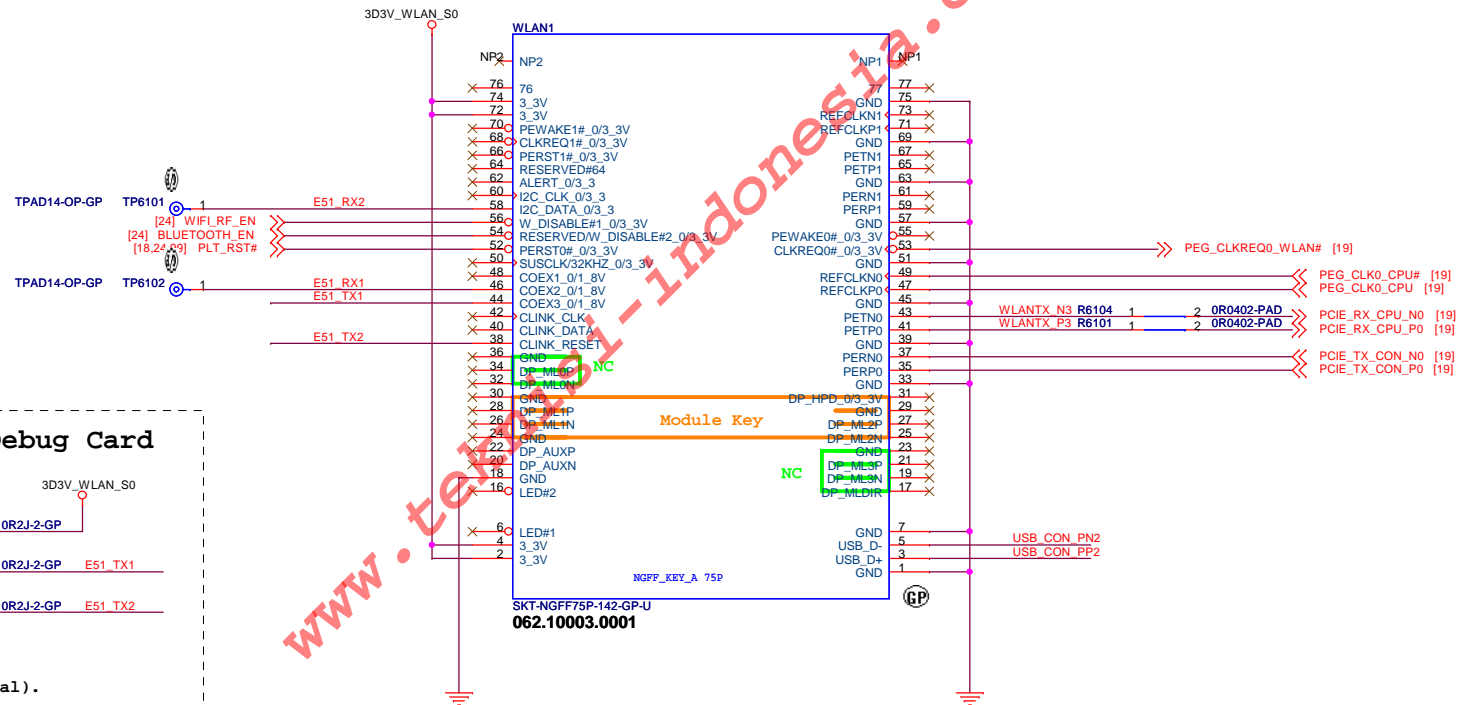
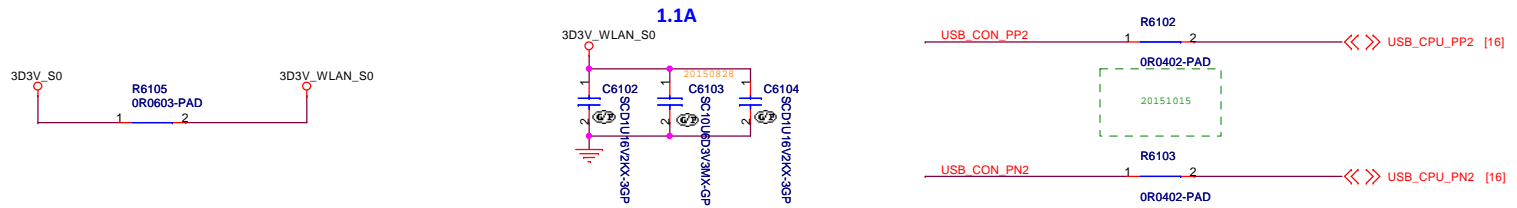
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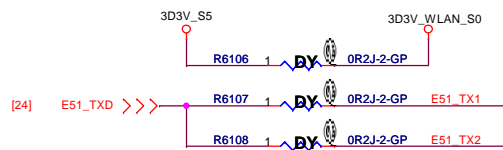
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SSID = WLAN

Mini Card Connector(802.11a/b/g)



Reserved for NGFF Debug Card



EE Note:
For NFGG Debug Card:
Stuff R6106,R6107,R6108(optional).
DY R6105

3D3V WLAN S0	1	AFTP6101
PEG CLKREQ0 WLAN#	1	AFTP6102
WIFI RF EN	1	AFTP6104
PLT RST#	1	AFTP6105
BLUETOOTH EN	1	AFTP6110
USB_CON PN2	1	AFTP6111
USB_CON PP2	1	AFTP6113

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SSID = WWAN

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(Reserved) WWAN

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SSID = SSD-NGFF

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Title

eMMC

Size

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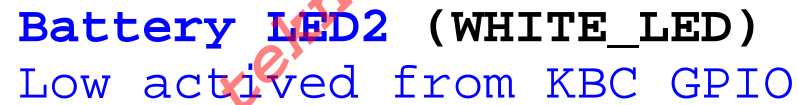
Sheet

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Battery LED1 (AMBER_LED)
Low activated from KBC GPIO

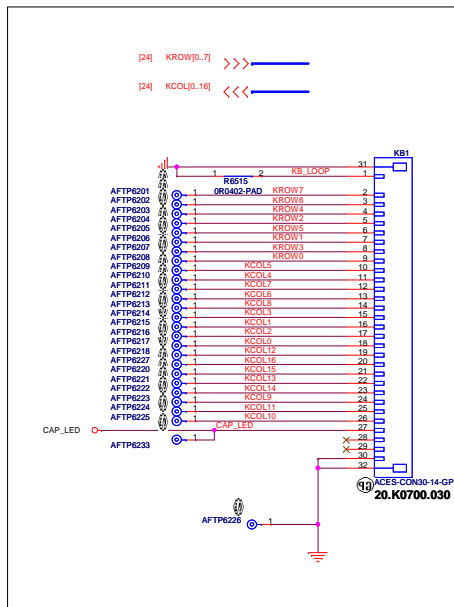
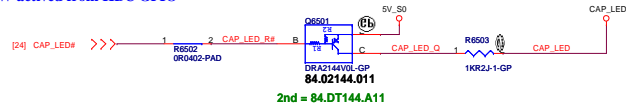


LED / PWRBTN

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CAP LED Control
LOW active from KBC GPIO

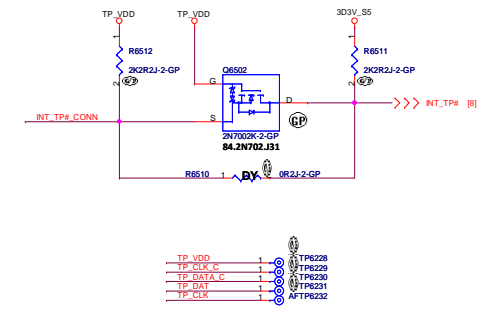
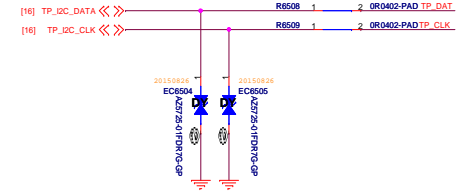
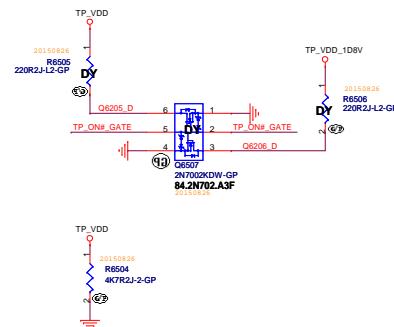
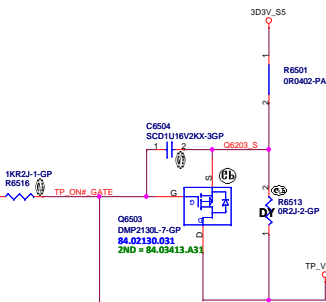
[24] KROW[0..7] >>>

[24] KCOL[0..16] <<<

CAP_LED EC8506 1 SC10P50V2JN-4GP

PIN#	SIGNAL
1	Diag_Loop=GPIO_1 (TPC)
2	KSI [7] = KBD S8
3	KSI [6] = KBD S7
4	KSI [4] = KBD S5
5	KSI [2] = KBD S3
6	KSI [5] = KBD S6
7	KSI [1] = KBD S2
8	KSI [3] = KBD S4
9	KSI [0] = KBD S1
10	KSO [5] = KBD D6
11	KSO [4] = KBD D5
12	KSO [7] = KBD D8
13	KSO [6] = KBD D7
14	KSO [8] = KBD D9
15	KSO [3] = KBD D4
16	KSO [1] = KBD D2
17	KSO [2] = KBD D3
18	KSO [0] = KBD D1
19	KSO [12] = KBD D13
20	KSO [16] = KBD D17
21	KSO [15] = KBD D16
22	KSO [13] = KBD D14
23	KSO [14] = KBD D15
24	KSO [9] = KBD D10
25	KSO [11] = KBD D12
26	KSO [10] = KBD D11
27	CapsLock LED
28	N/C
29	N/C
30	GND

[24] TP_ON# >>>



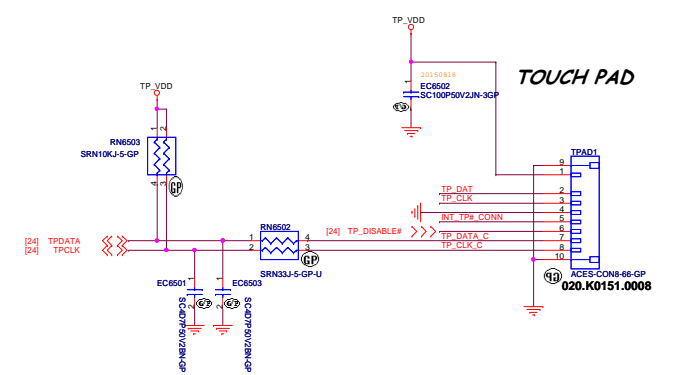
TP_VDD TP6228

TP_CLK C TP6229

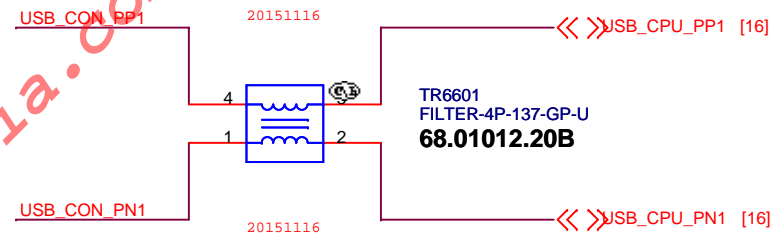
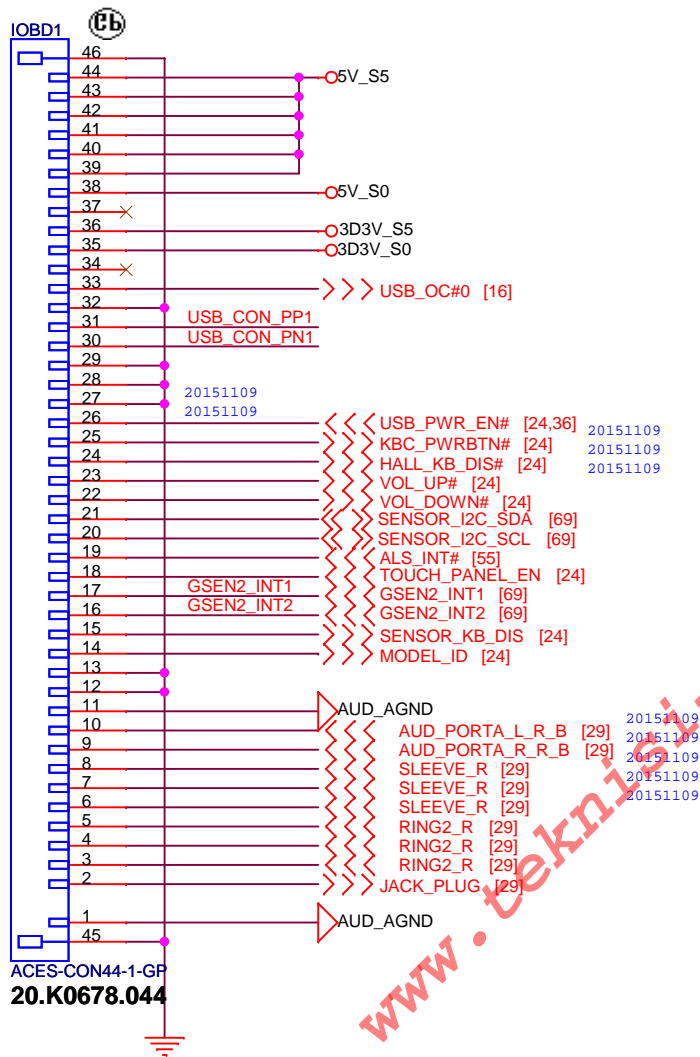
TP_DATA C TP6230

TP_DAT TP6231

TP_CLK AFTP6232



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Power Pin Count : 9
GND Pin Count : 8

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Title

IO Board CONN

Size
A4

Document Number

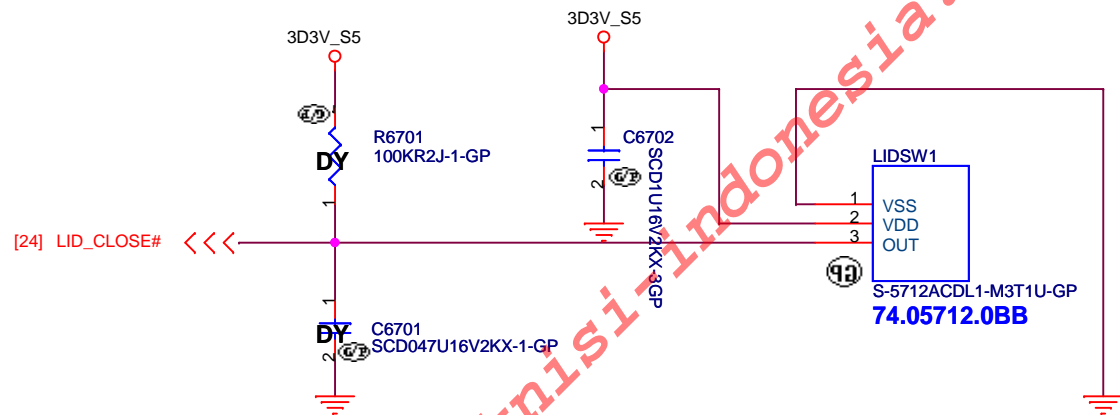
Rocket BSW 11.6"

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Title

Hall Sensor

Size
A4

Document Number

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SSID = Debug CONN

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Title

(Reserved) Debug CONN

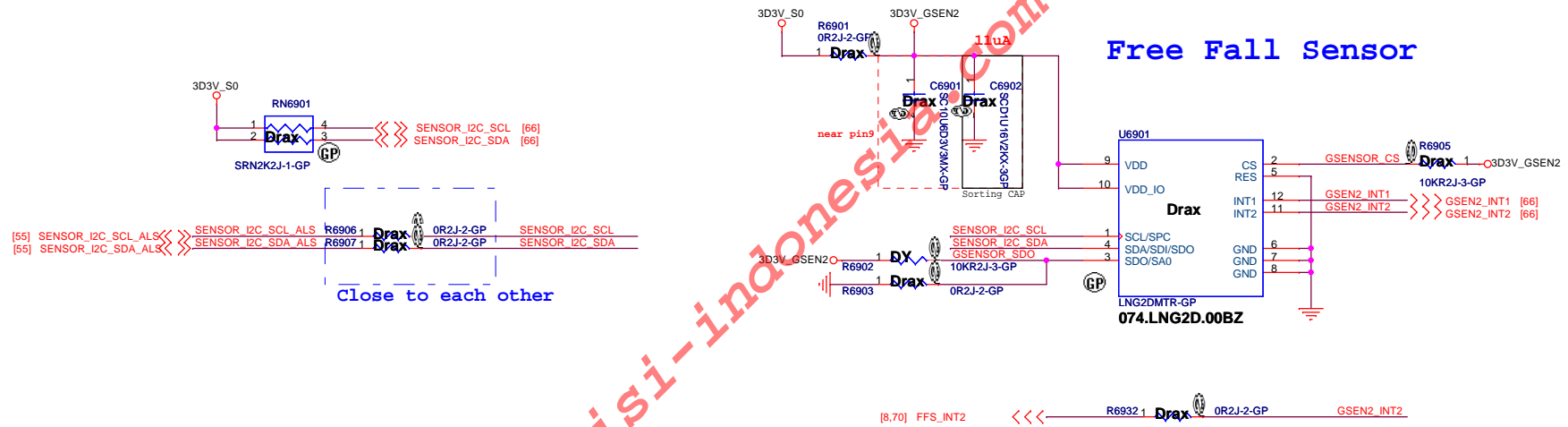
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Document Number
Rocket BSW 11.6"

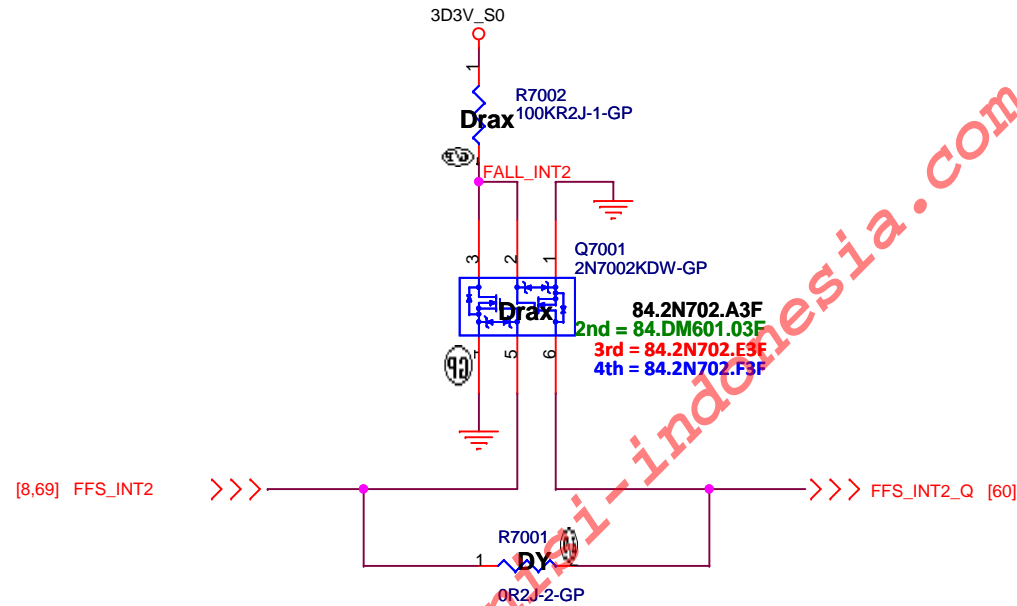
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SSID = Sensor



SSID = Free Fall Sensor



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DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Free Fall Sensor			
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Title **(Reserved)Thunderbolt (1/5)**

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Title **(Reserved)Thunderbolt (2/5)**

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Title **(Reserved)Thunderbolt (3/5)**

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Title **(Reserved)Thunderbolt (4/5)**

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Title **(Reserved)Thunderbolt (5/5)**

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Title **(Reserved)GPU (1/5) PEG**

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Title **(Reserved)GPU (2/5) DIGITAL**

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Title **(Reserved)GPU (3/5) VRAM**

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Title **(Reserved)GPU (4/5) GPIO**

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Title **(Reserved)GPU (5/5) PWR/GND**

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Title **(Reserved)VRAM1,2 (1/4)**

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Title **(Reserved)VRAM3,4 (2/4)**

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Title			(Reserved)VRAM5,6 (3/4)		
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Title **(Reserved)VRAM7,8 (4/4)**

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Title
(Reserved)VGA_CORE

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Title **(Reserved)DISCRETE VGAPOWER**

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34.43E24.001

SPRING-13-GP-U
SPR1



20151124

34.4YW18.001

SPRING-171-GP
SPR2



20150901

20151008

34.34S02.002

SPRING-98-GP
SPR4



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SPR6



20151008

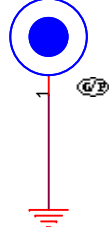
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SPR7



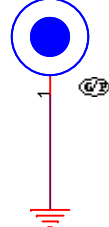
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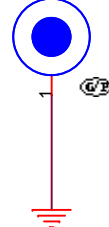
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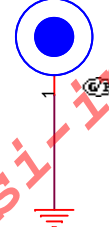
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HOLE335R197-GP



ZZ.00PAD.7L1

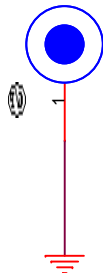
H9
HOLE335R197-GP



20151012 Remove H12 H14

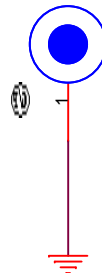
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HS1
STF237R117H67-3-GP



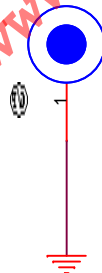
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HS2
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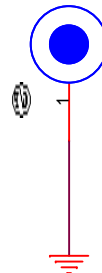
34.40X45.101

HS3
STF237R117H67-3-GP



34.40X45.101

HS4
STF237R117H67-3-GP



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Title

UNUSED PARTS/EMI Capacitors

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Title **(Reserved)NFC Connector**

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Title

(Reserved) TPM

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Title **(Reserved)Finger Print**

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(Reserved)Express Card

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Title			(Reserved)Smart Card Socket		
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Title **(Reserved)SW GFX eDP**

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Title **(Reserved)Bottom Docking**

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Title

(Reserved)LAN

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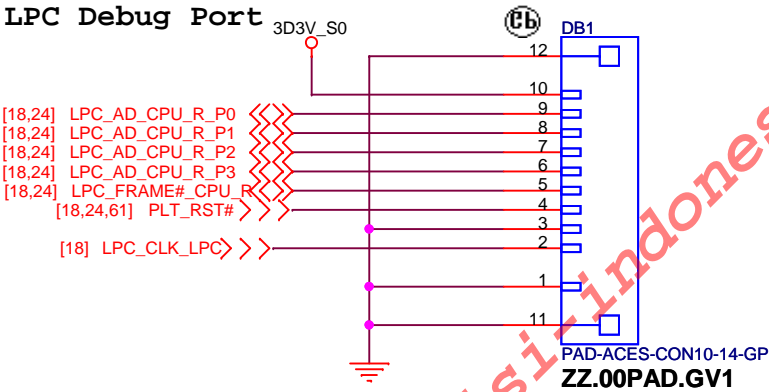
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Title **(Reserved)LAN SWITCH**

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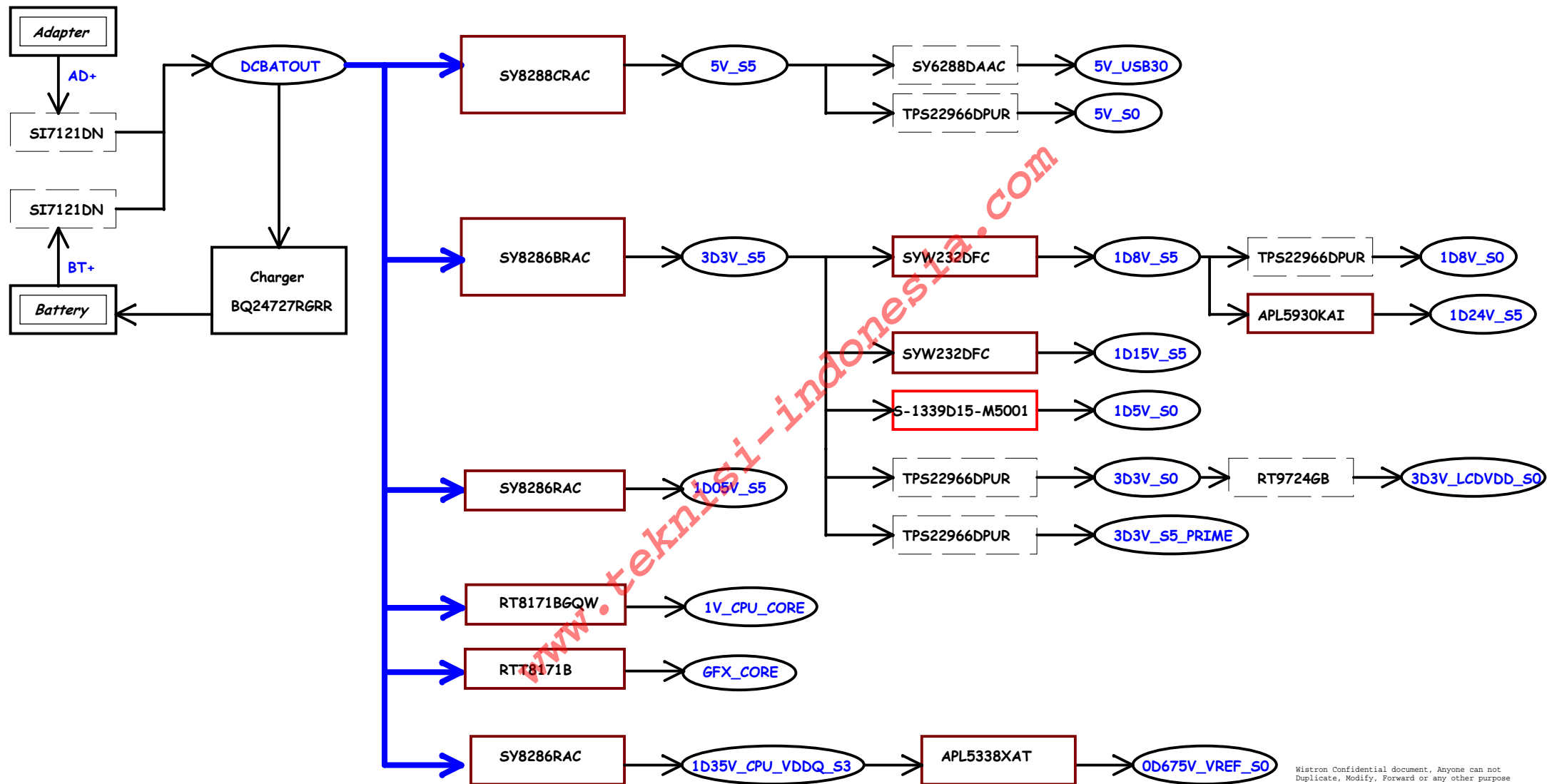
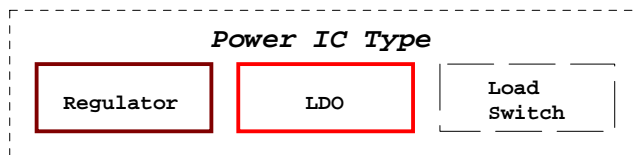
SSID = DEBUG PORT



20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
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CPU XDP					
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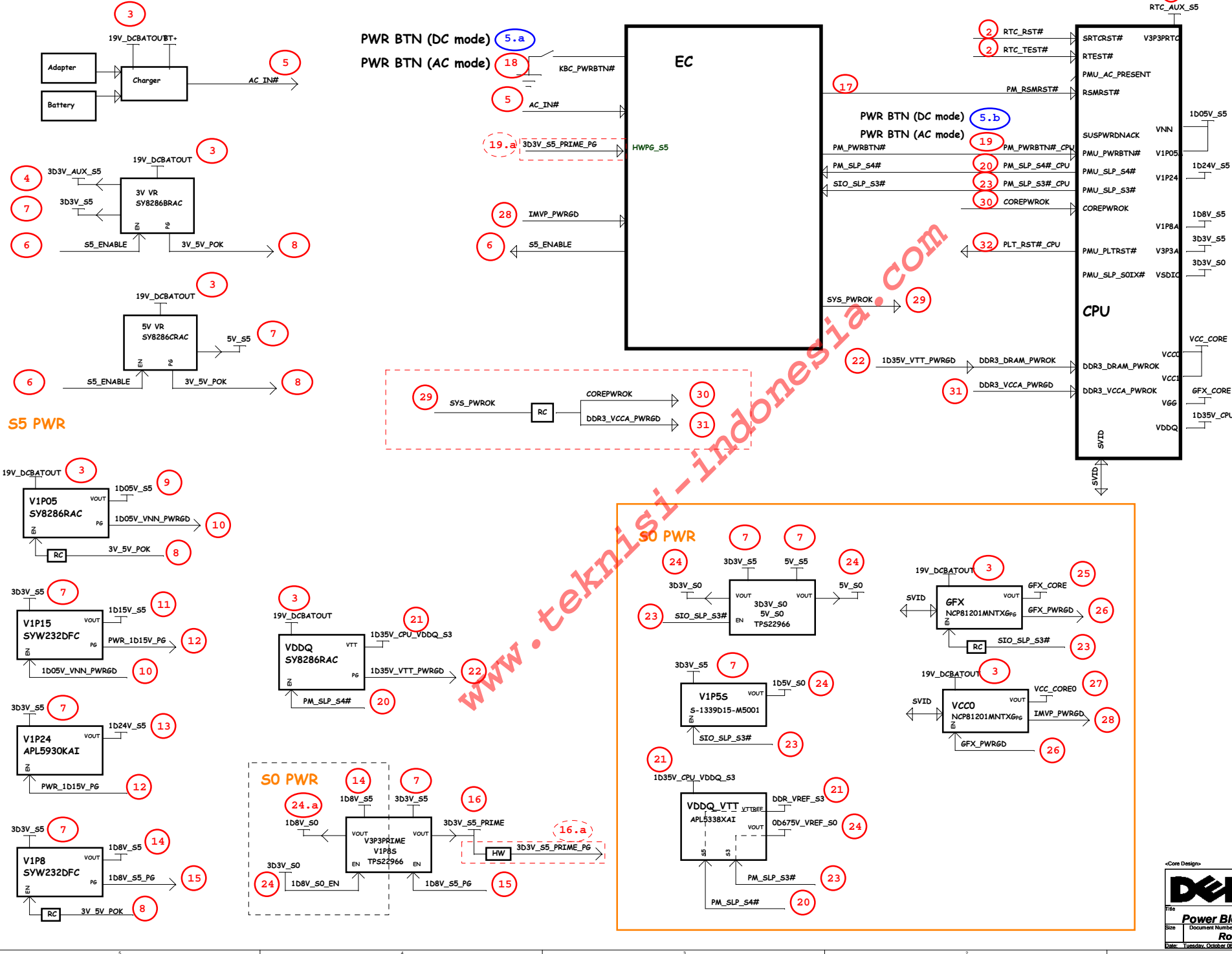
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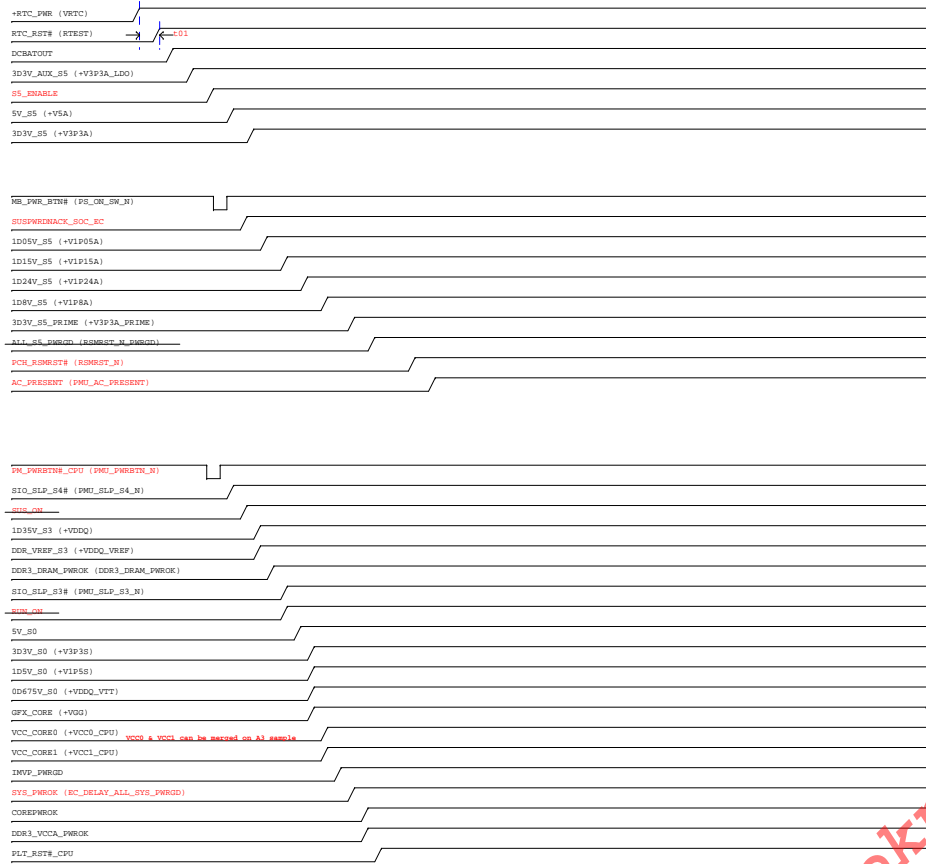
Title			Power Block Diagram	
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Braswell POWER UP SEQUENCE DIAGRAM



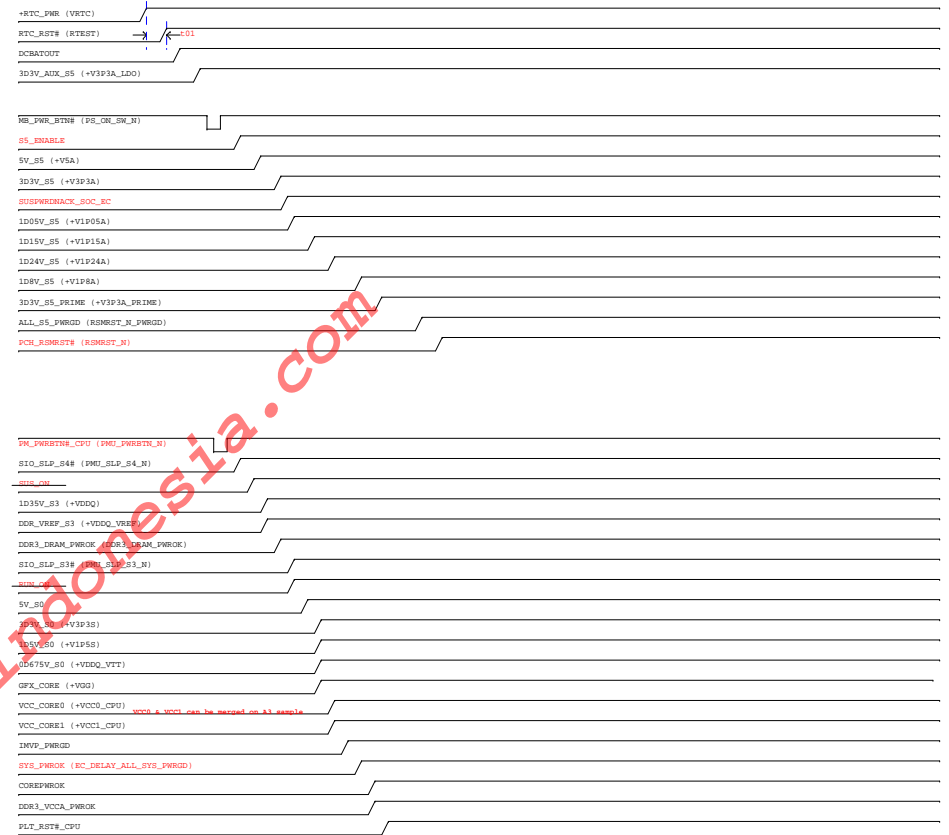
Intel-Power Up Sequence

(AC mode) Red word : RMC GP20



Intel-Power Up Sequence

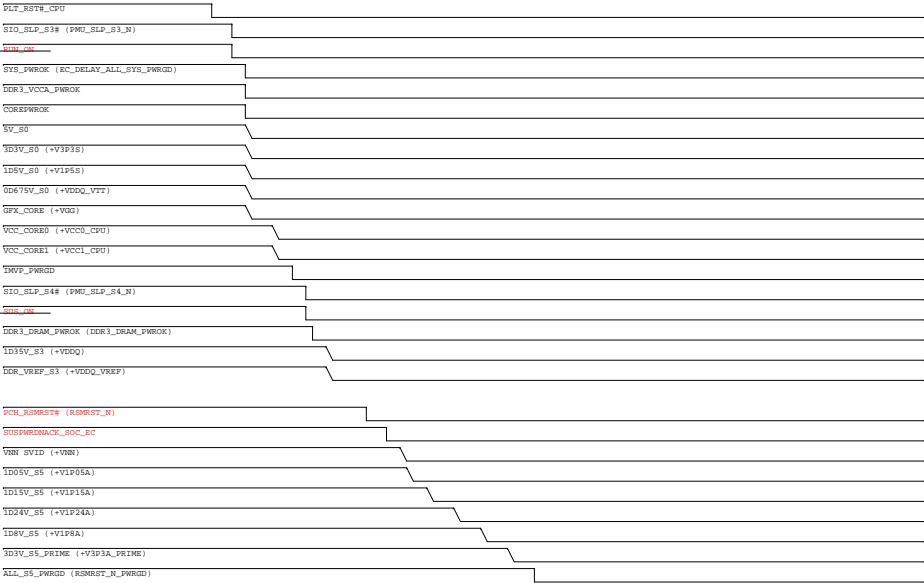
(DC mode) Red word : RMC GP20



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Intel-Power Down Sequence

(AC mode) Red word : KBC GPIO



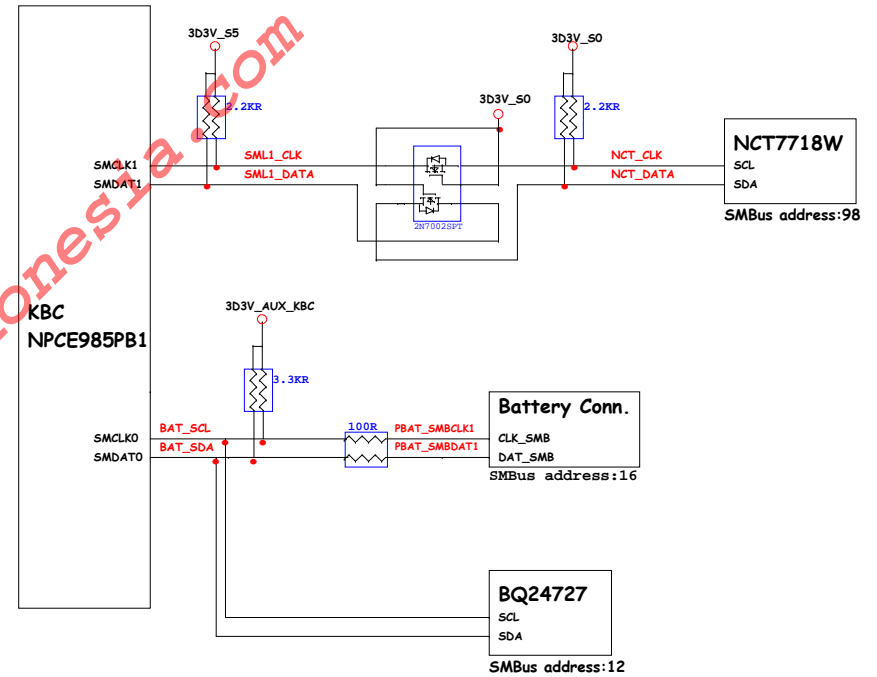
Intel-Power Down Sequence

(DC mode) Red word : KBC GPIO

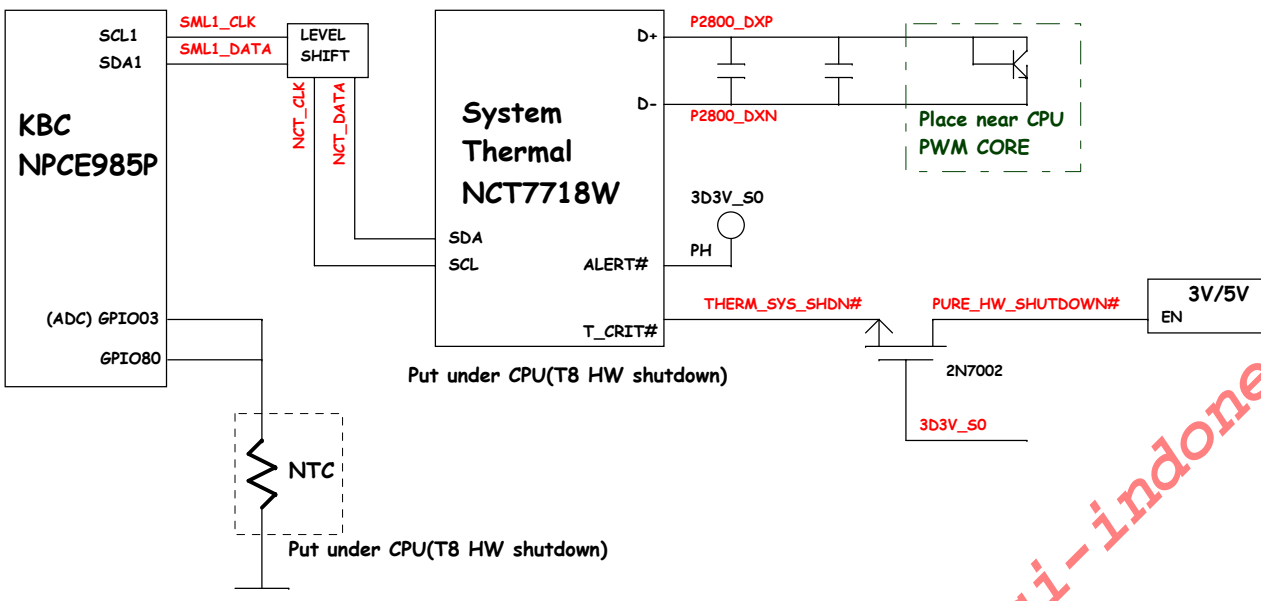


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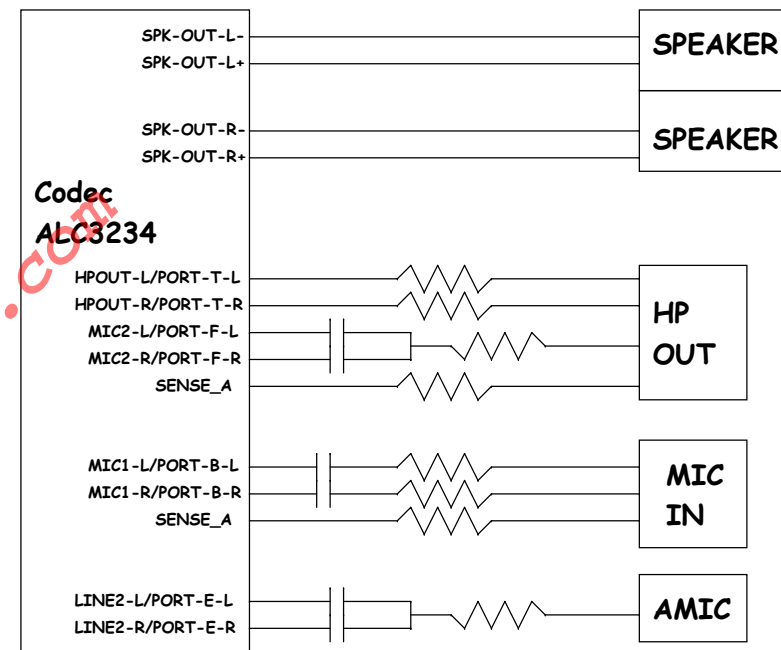
KBC SMBus Block Diagram



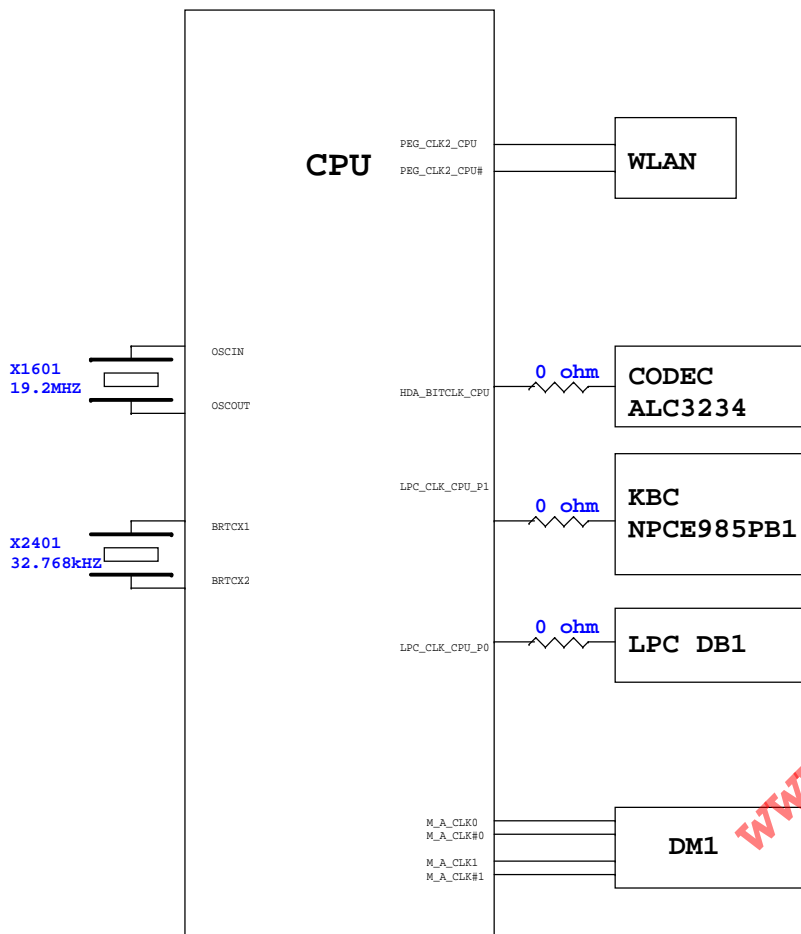
Thermal Block Diagram



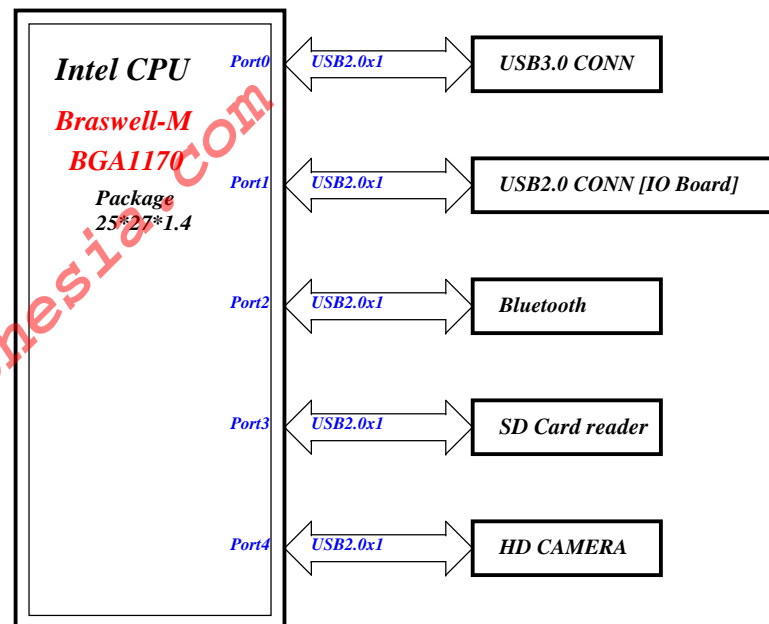
Audio Block Diagram



CLK Block Diagram



USB2.0 Port Block Diagram



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CLK / USB Block

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